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Single transistor primitive for timing and power modelling of CMOS gates

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An accurate and efficient method for modelling CMOS gates by a single equivalent transistor is introduced in this paper. The output waveform of a CMOS inverter is obtained by solving the circuit differential equation considering only the conducting transistor of the inverter. The effect of the short-circuiting transistor is incorporated as a differentiation of the width of the conducting transistor. The proposed model is the simplest primitive that can be used in order to obtain the propagation delay and short-circuit power dissipation of CMOS gates. Consequently, it can offer significant speed improvement to existing dynamic timing and power simulators while maintaining a sufficient level of accuracy.

1. Introduction

The demand for short development times of digital integrated circuits imposes the use of fast and accurate verification tools. It has been extensively pointed out that, with shrinking device dimensions and increasing number of transistors on integrated circuits in the submicron era, the difficulty in performing efficient simulation of these circuits is increasing. In contrast to numerical approaches such as SPICE, for calculating propagation delay and power dissipation, analytical methods can offer a significant speed improvement, on the assumption that accurate models which can describe the behaviour of transistor structures exist.

The simplest representation of static logic gates that has been presented in the literature is the equivalent inverter of a gate (Nabavi-Lishi and Rumin 1994, Kong *et al.* 1997, Chatzigeorgiou and Nikolaidis 1998, Chatzigeorgiou *et al.* 1999). If the width of the transistors in the equivalent inverter and other key points (Chatzigeorgiou *et al.* 1999) are calculated properly, the performance of complex gates can be estimated with very good accuracy by transient analysis of the equivalent inverter, thus enabling the timing and power analysis of digital integrated circuits at a lower level of complexity. In this way macromodels or accurate analytical techniques have to be developed only for the corresponding inverters (Kong and Overhauser 1995, Bisdounis *et al.* 1998, Hirata *et al.* 1998, Turgis and Auvergne 1998). However, the analysis at the inverter level remains complicated, mainly because of the presence of the short-circuit current and the nature of the differential equation that governs its operation, resulting in a relatively large runtime penalty (Kong and Overhauser 1995).

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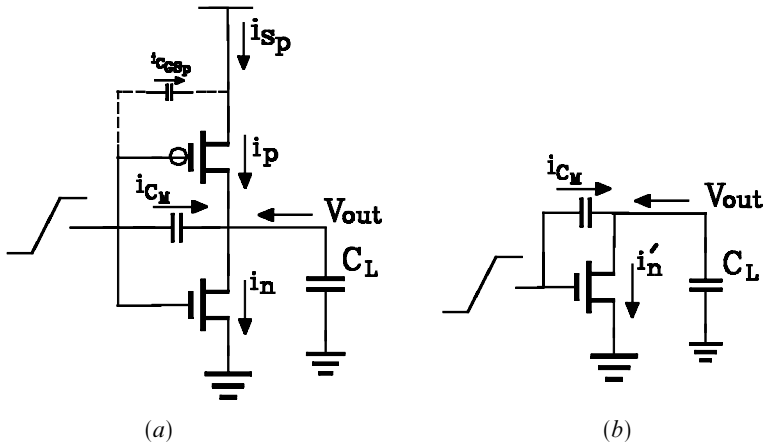
In this work the previous approach is extended in order to obtain a single transistor which models accurately the behaviour of an inverter. The output waveform is determined by solving the differential equation that describes the operation of the circuit considering only the conducting transistor. The question is how to incorporate in the analysis the effect of the short-circuit current. This current reduces the 'effective' charging/discharging output current, thus increasing the propagation delay as it slows down the output evolution. The effect of the short-circuit current can be considered from a different point of view as a differentiation (reduction) of the actual driving transistor width in order to charge or discharge the output load at a slower pace. The accurate calculation of the driving transistor width according to the region of operation of the short-circuiting device will be presented in the rest of the paper.

The use of a much simpler primitive for modelling CMOS gates reduces the computational complexity in two ways. First, the form of the differential equation becomes simpler and so, consequently, does the solution. Moreover, the differential equation of an inverter cannot be solved for some regions—being a Ricatti-like equation (Jeppson 1994)—thus imposing the use of many series approximations which increase the execution time and reduce the accuracy.

The rest of the paper is organized as follows. In § 2 the transistor width of the single transistor primitive is calculated, and in § 3 the output waveform expressions are derived. The short-circuit energy dissipated when the output of an inverter changes state is estimated in § 4 and in § 5 results of the proposed model are given. Finally, conclusions are drawn in § 6.

2. Single transistor width evaluation

Let us consider the inverter in figure 1(*a*) to which a rising input ramp with transition time τ is applied, and a single transistor driving the same load (figure 1(*b*)) whose width is to be calculated so that its output response matches that of the inverter when the same input is applied. The gate-to-drain coupling capacitance C_M is also shown in figure 1. For the equivalent transistor the coupling capacitance should take into account the gate-to-drain capacitances of both transistors. The



(*a*) (*b*)

Figure 1. (*a*) CMOS inverter and (*b*) single transistor primitive.

analysis focuses on the estimation of the width of the equivalent nMOS transistor for a rising input ramp. For the case of a falling input ramp the width of the equivalent pMOS is estimated in a symmetrical way.

The alpha power law model (Sakurai and Newton 1990), which takes into account the carrier velocity saturation effect of short-channel devices, will be used for the transistor currents since it combines accuracy and simplicity and is appropriate for modelling submicron devices (the equations correspond to the nMOS transistor):

$$I_{\mathrm{D}} = \begin{Bmatrix} 0 & V_{\mathrm{GS}} \le V_{\mathrm{TN}}: \text{cutoff region} \\ k_l(V_{\mathrm{GS}} - V_{\mathrm{TN}})^{\alpha/2} V_{\mathrm{DS}} & V_{\mathrm{DS}} < V_{\text{D-SAT}}: \text{linear region} \\ k_s(V_{\mathrm{GS}} - V_{\mathrm{TN}})^{a} & V_{\mathrm{DS}} \ge V_{\text{D-SAT}}: \text{saturation region} \end{Bmatrix} \tag{1}$$

where $V_{\text{D-SAT}}$ is the drain saturation voltage (Sakurai and Newton 1990), k_l, k_s are the transconductance parameters which depend on the width-to-length ratio of a transistor, α is the carrier velocity saturation index and V_{TN} is the threshold voltage.

The differential equations that govern the behaviour of the two circuits are

$$i_n - i_p = i_{C_M} - C_L \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} \quad \text{(inverter)} \tag{2}$$

$$i'_n = i_{C_{\mathrm{M}}} - C_{\mathrm{L}} \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} \quad \text{(equivalent transistor)} \tag{3}$$

where

$$i_{C_{\mathrm{M}}} = C_{\mathrm{M}} \left(\frac{\mathrm{d}V_{\mathrm{in}}}{\mathrm{d}t} - \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} \right)$$

is the current through the coupling capacitance between input and output.

Since the output response is the same for both circuits, it is

$$i'_n = i_n - i_p \tag{4}$$

Initially, the pMOS transistor operates in the linear region (since its V_{DS} is small) and the nMOS transistor, after it starts conducting, operates in saturation (since its V_{DS} is large). Thus, equation (4) can be written as

$$P_{s_n} \frac{W_x}{L} (V_{\mathrm{in}} - V_{\mathrm{TN}})^{a_n} = P_{s_n} \frac{W_n}{L} (V_{\mathrm{in}} - V_{\mathrm{TN}})^{a_n} - P_{l_p} \frac{W_p}{L} (V_{\mathrm{DD}} - V_{\mathrm{in}} - |V_{\mathrm{TP}}|)^{a_p/2} \times (V_{\mathrm{DD}} - V_{\mathrm{out}}) \tag{5}$$

from which the required width of the single equivalent transistor W_x can be found as a function of time t and V_{out}.

It has been observed that the time point at which the short-circuiting pMOS transistor of the inverter enters saturation, t_{s_p} (figure 2), is related to the time point when it ceases to conduct $(t_p = [(V_{\mathrm{DD}} - |V_{\mathrm{TP}}|)/V_{\mathrm{DD}}]\tau)$ by the equation $t_{s_p} = ht_p$ (Bisdounis *et al.* 1996). The empirical coefficient h depends on the quantity $G_{np} = [(I_{\mathrm{DO}_n} - 0.2I_{\mathrm{DO}_p})\tau]/(V_{\mathrm{DD}} C_{\mathrm{L}})$, which is a measure of the transconductance of the conducting path and determines how fast the output discharges. G_{np} depends on the drivability of the nMOS and pMOS devices (taking into account the fact that the short-circuit current is much smaller than the driving current). $I_{\mathrm{DO}_{n/p}}$ is the transistor drain current when $V_{\mathrm{GS}} = V_{\mathrm{DS}} = V_{\mathrm{DD}}$. G_{np} also takes into account the input waveform slope, the output load and the value of the supply voltage. In table 1 the values

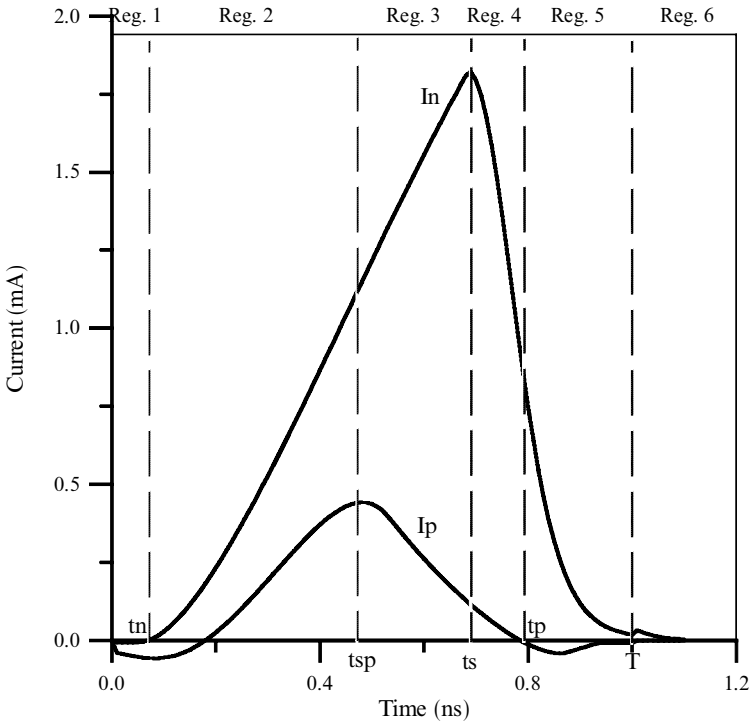


Figure 2. nMOS and pMOS currents of the inverter during output transition.

G_{np}	0.2–2.5	2.5–10	> 10
h	0.65	0.6	0.55

Table 1. Estimation of empirical parameter h.

of h depending on G_{np} are given for a 0.5 μm Hewlett Packard (HP) technology. This approximation has been tested on several inverter configurations and is also validated by the overall results.

Since t_{s_p} is known, the output voltage value at this time point can be calculated because at this point the values of the short-circuit currents in the linear region and in saturation become equal. It is

$$k_{l_p}\left(V_{\mathrm{DD}} - V_{\mathrm{in}}[t_{s_p}] - |V_{\mathrm{TP}}|\right)^{a_p/2}\left(V_{\mathrm{DD}} - V_{\mathrm{out}}\right) = k_{s_p}\left(V_{\mathrm{DD}} - V_{\mathrm{in}}[t_{s_p}] - |V_{\mathrm{TP}}|\right)^{a_p} \qquad (6)$$

from which the output voltage at t_{s_p} is obtained.

Since the nMOS transistor is still in saturation when the pMOS transistor exits the linear region (Bisdounis *et al.* 1998) the required value of W_x up to time point t_{s_p} can be found by substituting into equation (5) the value of V_{out} at t_{s_p}. This value of W_x will be referred to as W_1.

The next region for which the width of the single equivalent transistor should be calculated is up to time point t_p, since from t_{s_p} to t_p the pMOS transistor operates in saturation. Obviously, at time point t_p the calculated value of W_x would be equal to the nMOS transistor width of the actual inverter, W_n, since there is no short-circuit current at this point. Hence, the value of W_x in this region is selected as an average,

$W_2 = (W_1 + W_n)/2$. In the last region $(t > t_p)$, $W_x(W_3)$ is equal to W_n as no short-circuit current exists.

These three distinct W_x values are used in order to solve the differential equation that describes the operation of the single equivalent transistor in figure 1(*b*). Since the form of the differential equation (3) is simpler than that of the initial inverter, the solution and the resulting expressions for the output waveform are simpler and less time consuming.

3. Output waveform evaluation

Since the nMOS transistor can be either in saturation or in the linear region when the input reaches its final value, two major cases of input ramps will be considered (Bisdounis *et al.* 1998): for *fast* input ramps the nMOS device is still saturated whereas for *slow* input ramps the nMOS device is in the linear region when the input ramp reaches V_{DD}. Taking into account that three different transistor widths are being used, the bounds of the operating regions (figure 2) depend on the input transition time, the output load and the transistor widths. For the sake of simplicity a common pattern is analysed where the input ramp is slow.

The differential equation at the output of the single transistor primitive can be solved as follows.

3.1. *Region 1* $(t < t_n)$

In this region the single equivalent transistor is cut off since the input has not reached the nMOS transistor threshold voltage, V_{TN}. However, due to the coupling capacitance between input and output, C_M, a small overshoot on the output voltage appears. The differential equation at the output node becomes

$$C_M\left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt}\right) = C_L\frac{dV_{out}}{dt} \tag{7}$$

which has the solution

$$V_{out}[t] = V_{DD} + \frac{C_M}{C_L + C_M}\frac{V_{DD}}{\tau}t \tag{8}$$

The time point t_n occurs when $V_{in} = V_{TN}$ and therefore is equal to $t_n = (V_{TN}/V_{DD})\tau$.

It should be mentioned that, according to the proposed method the effect of the pMOS current during the overshoot of the output voltage has not been taken into account. In this region the pMOS current flows towards V_{DD}, thus 'removing' charge from the output load and helping the output to discharge (Bisdounis *et al.* 1998). However, the minimum pMOS value during the overshoot ($i_{p_{min}}$ in figure 3) is extremely small and, if we consider its effect negligible, does not have any impact on the overall accuracy of the method.

3.2. *Region 2* $(t_n < t < t_{s_p})$

The transistor operates in saturation and the equivalent transistor width according to the previous analysis is equal to W_1. The input ramp is in transition. Differential equation (3) becomes

$$P_{s_n}\frac{W_1}{L}\left(\frac{V_{\mathrm{DD}}}{\tau}t - V_{\mathrm{TN}}\right)^{a_n} = C_{\mathrm{M}}\left(\frac{V_{\mathrm{DD}}}{\tau} - \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t}\right) - C_{\mathrm{L}}\frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} \tag{9}$$

which has the solution

$$V_{\mathrm{out}}[t] = k_1 t - k_2 W_1\left[\frac{V_{\mathrm{DD}}}{\tau}t - V_{\mathrm{TN}}\right]^{a_n+1} + C_1 \tag{10}$$

where

$$k_1 = \frac{C_{\mathrm{M}}V_{\mathrm{DD}}}{(C_{\mathrm{L}}+C_{\mathrm{M}})\tau}, \qquad k_2 = \frac{P_{s_n}\tau}{(C_{\mathrm{L}}+C_{\mathrm{M}})(1+\alpha_{\mathrm{n}})V_{\mathrm{DD}}L}$$

and C_1 is the integration constant.

3.3. *Region 3* $\left(t_{s_p} < t < t_s\right)$

The transistor operates in saturation up to time point t_s when it enters the linear region, and the transistor width is now equal to W_2 since the pMOS transistor has entered saturation. The output waveform is given by

$$V_{\mathrm{out}}[t] = k_1 t - k_2 W_2\left[\frac{V_{\mathrm{DD}}}{\tau}t - V_{\mathrm{TN}}\right]^{a_n+1} + C_2 \tag{11}$$

where C_2 is the integration constant.

Time point t_s can be found by equating the actual drain to source voltage of the transistor to the drain saturation voltage (Sakurai and Newton 1990):

$$V_{\mathrm{out}}[t_s] = V_{\text{D-SATN}}[t_s] \Rightarrow k_1 t - k_2 W_2\left[\frac{V_{\mathrm{DD}}}{\tau}t - V_{\mathrm{TN}}\right]^{a_n+1} + C_2 = \frac{P_{s_n}}{P_{l_n}}\left[\frac{V_{\mathrm{DD}}}{\tau}t - V_{\mathrm{TN}}\right]^{a_n/2} \tag{12}$$

which can be solved analytically using first order Taylor series approximation around $t = \tau/2$ for the terms which are powered to $(a_n + 1)$ and $a_n/2$.

3.4. *Region 4* $\left(t_s < t < t_p\right)$

The transistor operates in the linear region and its width is equal to W_2. Since the input ramp is still in transition the differential equation at the output node is

$$P_{l_n}\frac{W_2}{L}\left(\frac{V_{\mathrm{DD}}}{\tau}t - V_{\mathrm{TN}}\right)^{a_n/2} V_{\mathrm{out}} = C_{\mathrm{M}}\left(\frac{V_{\mathrm{DD}}}{\tau} - \frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t}\right) - C_{\mathrm{L}}\frac{\mathrm{d}V_{\mathrm{out}}}{\mathrm{d}t} \tag{13}$$

Neglecting the influence of the input ramp on the current through the input-to-output coupling capacitance (Bisdounis *et al.* 1998) the solution becomes

$$V_{\mathrm{out}}[t] = C_3 \exp\left[-k_3 W_2\left(\frac{V_{\mathrm{DD}}}{\tau}t - V_{\mathrm{TN}}\right)^{1+a_n/2}\right] \tag{14}$$

where

$$k_3 = \frac{2P_{l_n}\tau}{(C_{\mathrm{L}}+C_{\mathrm{M}})(2+a_n)LV_{\mathrm{DD}}}$$

and C_3 is the integration constant.

3.5. *Region 5* $(t_p < t < \tau)$

The pMOS transistor is cut off and consequently the equivalent transistor width is equal to $W_3 = W_n$. The solution is similar to that of the previous region

$$V_{\text{out}}[t] = C_4 \exp\left[-k_3 W_3 \left(\frac{V_{\text{DD}}}{\tau} t - V_{\text{TN}}\right)^{1+a_n/2}\right] \tag{15}$$

3.6. *Region 6* $(t > \tau)$

The input has reached its final value, the equivalent transistor is in the linear region and the pMOS device is cut off. The differential equation becomes

$$P_{l_n} \frac{W_3}{L} (V_{\text{DD}} - V_{\text{TN}})^{a_n/2} V_{\text{out}} = -(C_{\text{L}} + C_{\text{M}}) \frac{\mathrm{d}V_{\text{out}}}{\mathrm{d}t} \tag{16}$$

which has the solution

$$V_{\text{out}}[t] = C_5 \exp[-k_4 W_3 t] \tag{17}$$

where

$$k_4 = \frac{P_{l_n} (V_{\text{DD}} - V_{\text{TN}})^{a_n/2}}{(C_{\text{L}} + C_{\text{M}}) L}$$

and C_5 is the integration constant.

According to this analysis, the output waveform of a CMOS inverter can be obtained with very good accuracy. Results of the proposed method are given in § 5.

4. Short-circuit power dissipation

During the output switching of a CMOS inverter and while both nMOS and pMOS transistors are conducting, a path from V_{DD} to ground exists and causes short-circuit power dissipation. Since the output waveform has been obtained, the form and the magnitude of the pMOS current can be estimated in order to calculate the short-circuit energy which is dissipated when the output of an inverter switches state.

However, the current that is causing the short-circuit power dissipation, i_{s_p}, is not the pMOS transistor current but the current that is flowing from V_{DD} towards the source of the pMOS transistor (Nikolaidis and Chatzigeorgiou 1999) (figure 1(*a*)). In order to calculate this current, Kirchhoff's current law has to be applied at the source node of the pMOS transistor, which gives

$$i_{s_p} = i_p - i_{C_{\text{GS}_p}} \tag{18}$$

where $i_{C_{\text{GS}_p}} = C_{\text{GS}_p}(\mathrm{d}V_{\text{in}}/\mathrm{d}t) = C_{\text{GS}_p}(V_{\text{DD}}/\tau)$ is the current through the gate-to-source coupling capacitance of the pMOS transistor. Since the gate-to-source capacitance has two different values, $C_{\text{GS}_1} = \frac{1}{2} C_{\text{ox}} WL$ in the linear region and $C_{\text{GS}_2} = \frac{2}{3} C_{\text{ox}} WL$ in saturation, where C_{ox} is the gate capacitance per unit area (Rabaey 1996), two values will be used for $i_{C_{\text{GS}_p}}$ according to the time point t_{s_p} (figure 3).

The pMOS current can be approximated by a piece-wise linear function of time (Hirata *et al.* 1998) as shown in figure 3. It presents initially an undershoot due to the

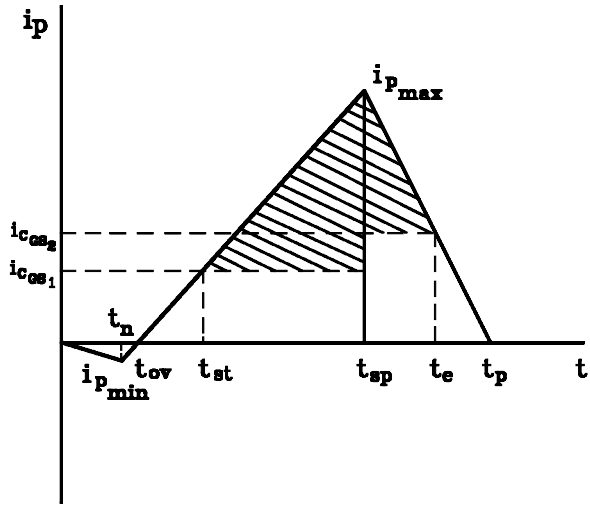


Figure 3. Representation of the pMOS transistor short-circuit current.

coupling capacitance between input and output which in turn causes an overshoot in the output voltage, forcing the output node of the inverter to be at a higher potential than V_{DD} (Bisdounis *et al.* 1998, Hirata *et al.* 1998, Nikolaidis and Chatzigeorgiou 1999). During the overshoot, current is flowing towards V_{DD}, causing the undershoot of the pMOS current. The minimum pMOS current occurs close to $t = t_n$ when current starts flowing through the nMOS transistor. The time point when the undershoot of the pMOS current or correspondingly the overshoot of the output voltage ceases, t_{ov}, can be calculated analytically by setting $V_{\mathrm{out}} = V_{\mathrm{DD}}$ in region 2.

The pMOS current is considered to cease at time point t_p whereas its maximum value, $i_{p_{\max}}$, occurs when the pMOS transistor enters saturation at time point t_{s_p} which is known and therefore $i_{p_{\max}} = k_{s_p}\left(V_{\mathrm{DD}} - V_{\mathrm{in}}[t_{\mathrm{sp}}] - V_{\mathrm{TP}}\right)^{a_p}$. Consequently, the pMOS current can be expressed by the following equations

$$i_p = \frac{i_{p_{\max}}}{t_{sp} - t_{\mathrm{ov}}}\left(t - t_{\mathrm{ov}}\right) \qquad t_{\mathrm{ov}} < t < t_{sp} \tag{19}$$

$$i_p = i_{p_{\max}} - \frac{i_{p_{\max}}}{t_p - t_{sp}}\left(t - t_{sp}\right) \qquad t_{sp} < t < t_p \tag{20}$$

Energy starts being dissipated at time t_{st} when i_{s_p} starts flowing towards the source of the pMOS transistor (Nikolaidis and Chatzigeorgiou 1999) so that a current path between V_{DD} and ground exists. Time t_{st} can be calculated by setting $i_{s_p} = 0$ in equation (18) and using the linear approximation for the pMOS current, as shown in figure 3. Thus

$$t_{st} = t_{\mathrm{ov}} + \frac{t_{sp} - t_{\mathrm{ov}}}{i_{p_{\max}}} \cdot i_{C_{\mathrm{GS}_1}}$$

Energy dissipation ceases at time point t_e when $i_s = 0$, after time t_{sp}. t_e is again calculated using the linear approximation for the pMOS current resulting in

$$t_e = t_p - \frac{t_p - t_{sp}}{i_{p_{\max}}} \cdot i_{C_{\mathrm{GS}_2}}$$

The short-circuit energy dissipated during output discharging is calculated as

$$E_{sc}^{d} = V_{DD}\left(\int_{t_{st}}^{t_{sp}} i_{s_p}\,dt + \int_{t_{sp}}^{t_e} i_{s_p}\,dt\right)$$

$$= \frac{1}{2}V_{DD}[(t_{sp}-t_{st})(i_{p_{max}} - i_{C_{GS_1}}) + (t_e - t_{sp})(i_{p_{max}} - i_{C_{GS_2}})] \qquad (21)$$

The short-circuit energy dissipated during output charging, E_{SC}^{c}, can be obtained in a symmetrical way.

Consequently, the short-circuit energy dissipation during a complete transition at the output node $[0 \to 1 \to 0]$ is $E_{sc} = E_{sc}^{c} + E_{sc}^{d}$ and the corresponding power can be calculated simply by multiplying the calculated energy by the frequency of transitions at the output of the gate.

5. Results

Results of the proposed method are given in figure 4 in which the output waveform of an inverter and that of its equivalent single transistor primitive are plotted for a 0.5 μm ($W_n = 4\,\mu m$, $W_p = 6\,\mu m$, $C_L = 100\,fF$) and a 0.35 μm ($W_n = 2.8\,\mu m$, $W_p = 4.2\,\mu m$, $C_L = 100\,fF$) HP technology for two different input transition times. The accuracy of the proposed method in the evaluation of the output waveform is obvious.

The propagation delay in CMOS gates is defined as the time from the half-V_{DD} point of the input to the half-V_{DD} point of the output waveform (Hedenstierna and Jeppson 1987). Propagation delays of a CMOS inverter ($W_n = 4\,\mu m$, $W_p = 6\,\mu m$, $L = 0.5\,\mu m$) have been calculated according to the proposed method for several input transition times and output loads and compared to simulated propagation delays using SPICE as shown in table 2.

The short-circuit energy for a single output transition calculated, according to the method of the previous section, lies very close to the energy measured from SPICE

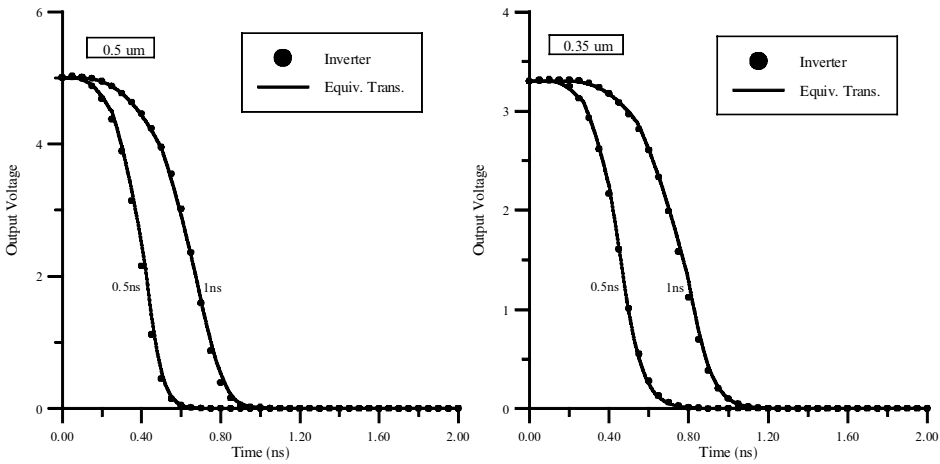


Figure 4. Output waveform of the CMOS inverter and the single equivalent transistor for two submicron technologies. The input transition time to which each output corresponds is also shown.

τ (ns)	C_L (fF)	Propagation delay, SPICE (ns)	Propagation delay, calculated (ns)	Error (%)
0.5	50	0.076	0.070	7.89
0.5	100	0.129	0.137	6.20
1	50	0.061	0.066	8.20
1	100	0.138	0.135	2.17
2	100	0.113	0.101	10.62
2	200	0.263	0.289	9.89

Table 2. Comparison between simulated and calculated propagation delays (0.5 μm).

simulations. In figure 5 a comparison of the calculated and simulated short-circuit energy values during output discharging of a CMOS inverter with $W_n = 4\,\mu m$, $W_p = 6\,\mu m$ and a 0.5 μm HP technology is shown for several input transition times and output loads. Using SPICE, the short-circuit power dissipation can be obtained by integrating the current at the source terminal of the pMOS transistor or by using a power meter (Kang 1986).

A tool that implements the proposed technique and another one that implements the fully analytical method presented in Bisdounis *et al.* (1998) has been developed. The execution time for the proposed method has been measured for several input transition times and output loads. On average, a speedup of 70 times compared to SPICE execution time has been found for a 0.5 μm technology, while an average speedup of 300 times compared to HSPICE for a 0.35 μm technology has been observed. Compared to the fully analytical method where both the pMOS and nMOS currents are taken into account in the solution of the circuit differential equation, the proposed method was found to be about 8 times faster on average.

Consequently, the proposed technique can offer a significant speed improvement if it is incorporated into existing dynamic timing simulators. In order to model CMOS circuits, methods have been developed (Kong *et al.* 1997, Chatzigeorgiou *et al.* 1999) for collapsing a complex CMOS gate to an equivalent NAND/NOR gate and then reducing such a gate to an equivalent inverter. This modelling process could be further enhanced by employing the proposed method to map an inverter to a

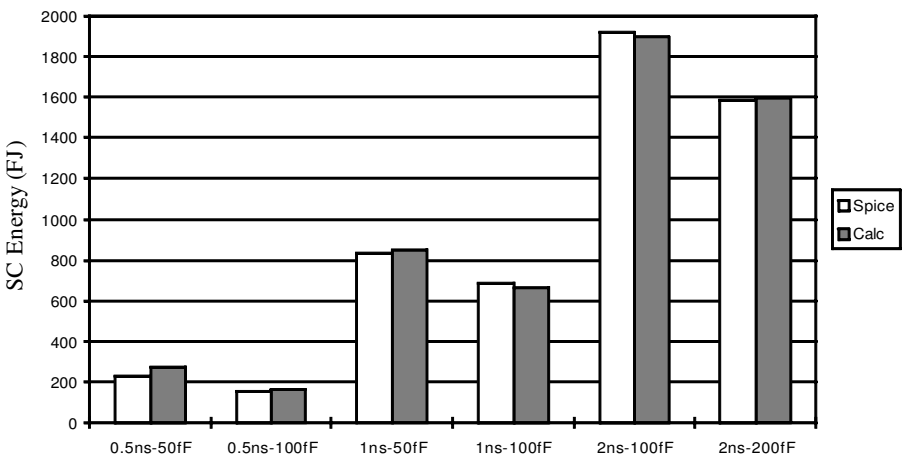


Figure 5. Simulated and calculated short-circuit energy dissipation.

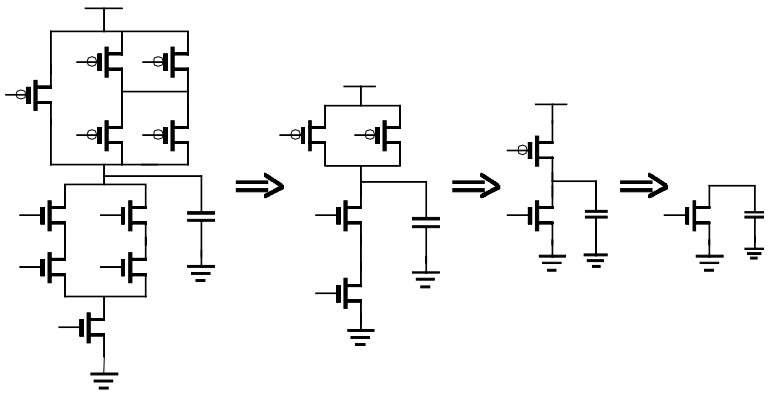


Figure 6. Mapping process for modelling of CMOS gates.

single transistor primitive. Such a process is shown diagrammatically in figure 6 and simplifies significantly the simulation of large circuits.

6. Conclusion

A method for modelling a CMOS inverter by a single equivalent transistor has been introduced in this paper. The width of the equivalent transistor is calculated according to the actual operating conditions of the conducting and the short-circuiting transistor so that the output response to an input ramp matches that of the actual inverter. In this way it is possible to perform the transient analysis of an inverter at a lower level of complexity, thus offering a significant speedup. The results prove that, according to the proposed method, the output waveform, the propagation delay and the short-circuit power dissipation of an inverter can be calculated with very good accuracy.

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