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Modelling the operation of pass transistor and CPL gates

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Pass transistor logic and complementary pass-transistor logic (CPL) are becoming increasingly important in the design of a specific class of digital integrated circuits owing to their speed and power efficiency as compared with conventional CMOS logic. In this paper, a simple and very accurate technique for the timing analysis of gates that involve pass transistor logic is presented. This investigation offers for the first time the possibility of simulating pass transistor and CPL gates by partitioning the behaviour of complex structures into well defined subcircuits whose interaction is studied separately. Using the proposed analysis, which is validated by results for two submicron technologies, most pass-transistor logic styles can be modelled efficiently. Consequently, a significant speed advantage can be gained compared with simulation tools that employ numerical methods such as SPICE.

1. Introduction

The intense and increasing demand for high performance and low power electronic devices has shifted the interest of the research community to the investigation and development of appropriate design techniques. This problem has been addressed at all levels of the design hierarchy such as the architectural, circuit, layout and the process technology level (Chandrakasan and Brodersen 1995). At the circuit level, significant power savings can be achieved by the selection of the proper logic style or by the development of new ones. Pass transistor logic (PTL) and especially complementary pass transistor logic (CPL) have become popular since they offer the possibility to implement high speed and low power circuits in certain applications. The popularity of these logic styles is indicated by the large number of circuits developed recently with increased performance in terms of speed and power efficiency (Yano *et al.* 1990, Suzuki *et al.* 1993, Ko *et al.* 1995, Abu-Khater *et al.* 1996, Law *et al.* 1999). In addition, during the past few years research has also focused on the development of synthesis methodologies that target pass transistor implementations starting from technology-independent descriptions such as hardware description languages (HDLs) (Yano *et al.* 1996, Ferrandi *et al.* 1998, Jaekel *et al.* 1998, Zhuang *et al.* 1999).

Generally, the use of PTL leads to reduced transistor count and smaller node capacitances thus decreasing the required area, rise/fall times and power dissipation. However, this circuit style presents the inherent problem of the threshold drop across a transistor which causes static power dissipation in the following stages and imposes the addition of level restoring transistors.

Although CPL is relatively expensive for simple monotonic gates it is appropriate and efficient in terms of transistor count for designs that employ the XOR and MUX

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operation. CPL presents the following advantages (Rabaey 1996, Zimmermann and Fichtner 1997). Logic is ratioless and high noise margins enable reliable operation even at low voltages. CPL gates present a good output driving capability owing to the output inverters and a fast differential stage owing to the cross-coupled pMOS pull-up transistors. Moreover, small input loads reduce the overall capacitance switched and consequently power consumption is lower and rise/fall times are faster. As an example, this aspect of CPL is attractive in high-performance applications such as multipliers (Yano *et al.* 1990).

From the implementation point of view, the efficient design of digital integrated circuits depends strongly on electronic design automation (EDA) tools that can estimate their performance quickly and accurately. Since the transistor count on integrated circuits is increasing there is an intense need for modelling techniques that can offer sufficient accuracy at times that are orders of magnitude smaller than the times required by tools that are based on numerical methods, such as SPICE.

In the recent literature extensive research results for the modelling of static CMOS gates (Hedenstierna and Jeppson 1987, Sakurai and Newton 1990, Kong *et al.* 1997, Bisdounis *et al.* 1998, Chatzigeorgiou *et al.* 1999, Nikolaidis and Chatzigeorgiou 1999) can be found. Methods have been developed for the calculation of the output waveform and the propagation delay of a CMOS gate in order to perform timing analysis of large integrated circuits.

However, very few modelling techniques for pass transistor or CPL gates can be found in the literature. These include a simplified analysis of a single pass transistor driven by a step input (Kang and Leblebici 1996) and a delay-macromodelling technique for transmission gates driven by a register cell operating in synchronous or asynchronous mode which has been developed by Vemuru (1995). The lack of modelling techniques for such gates is probably due to the fact that PTL and especially CPL gates have received increased attention only recently and because they employ more complicated structures in terms of analysis since they include transistors with floating terminals and no connections to power rails. Moreover, these pass transistors can receive a large number of input patterns which determine their operation, prohibiting the development of analytical methods for the estimation of the output waveform and the propagation delay.

In this paper a novel attempt to model pass transistor and CPL is presented. The basic idea behind the proposed approach is that CPL gates can be partitioned into subcircuits that can be modelled in a much simpler way. The interference between these subcircuits is incorporated as a separate step. It should be mentioned that in the following analysis semi-empirical or empirical techniques are often used instead of fully analytical methods. This has been done for two reasons. First, a mathematical analysis for all cases would lead to high complexity prohibiting the development of efficient design automation tools that could employ these methods. For example, the evaluation of the output waveform by means of the solution of differential equations is avoided (except for some simplified cases) since this approach would lead to a large number of solutions according to the applied input pattern. The second reason is that the operation of pass transistor logic is subject to specific rules which allow with sufficient accuracy the extraction of the output waveform of a gate by relating it to the input signals and adjusting their slope and/or delay.

Although the proposed methods concentrate on CPL, most logic styles that employ pass-transistor structures can be modelled efficiently by applying the proposed technique, since the same kind of modelling problems are present. Such logic

styles include double pass-transistor logic (DPL), single-rail pass-transistor logic (LEAP), differential pass-transistor logic (DPTL) and push–pull pass-transistor logic (PPL).

An overview of the strategy that is being followed to handle PTL is presented in § 2 and in § 3 the techniques to obtain the output waveform of a NAND2 CPL gate are described. Sections 4 and 5 discuss modelling of more complex pass transistor structures and finally we conclude in § 6.

2. Strategy of analysis

Since the problem of estimating the output waveform of a CPL gate may become extremely complicated, the strategy that is being followed is to partition a CPL gate into distinct and well defined subcircuits that can be modelled accurately.

Let us consider the example of a NAND2 gate implemented in CPL (Zimmermann and Fichtner 1997) which is shown in figure 1(*a*). The NAND2 gate is selected for the analysis because it forms a basic structure where most of the characteristics of pass transistor logic can be studied. It will be shown later that other CPL gates can be modelled using the same methodology. The NAND2 gate consists of two nMOS networks corresponding to two signal rails. Each network is driving an output inverter which provides the gate output signal. As observed, the two networks (which are separated by the horizontal dashed line in the figure) are symmetrical and each network consists of two pass transistors which are controlled by complementary input signals A and $\bar{A}$. One pass transistor is driven by an inverter that belongs to the gate of the preceding stage while the other pass transistor is either tied to ground or V_{DD}. As shown in figure 1, the two symmetrical networks receive complementary input signals B and $\bar{B}$. Each network is coupled with a pMOS transistor which receives as gate signal the output of the symmetrical network. The purpose of this pMOS transistor is to restore the level of the output signal, which in the case of a high output for the nMOS pass transistor is degraded due to

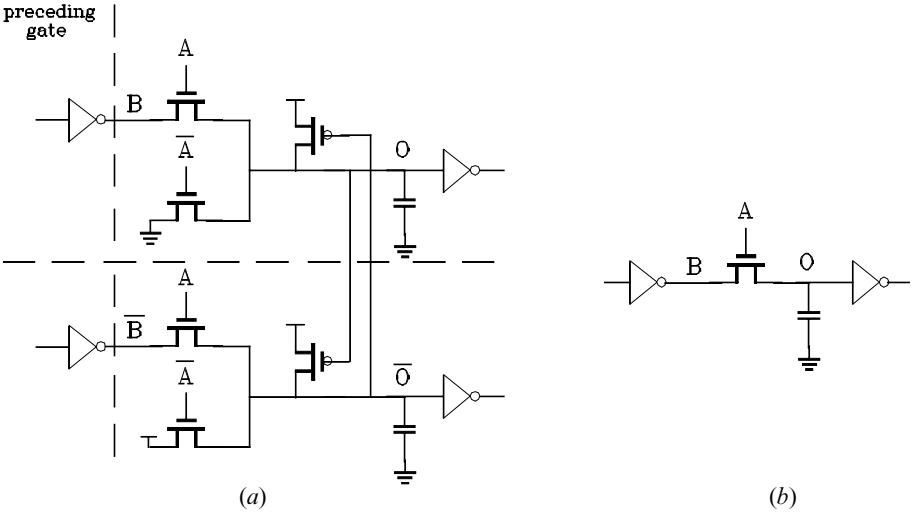


Figure 1. (*a*) NAND2 CPL gate and (*b*) pass transistor driven by inverter.

threshold drop back to the nominal V_{DD} value and therefore it is called a level restoring or pull-up transistor.

Each one of these nMOS networks is studied independently. The analysis for each network starts from the part of the circuit which is activated by the output of the preceding stage and once the output waveform is determined, the effect of all other parts of the circuit are gradually incorporated in the analysis. The effect of the pull-up transistors will be taken into account separately in the process of evaluating the output waveform of the CPL gate. Once the nMOS network output is obtained, the gate output is calculated by performing the analysis of the output inverter according to Bisdounis *et al.* (1998), Deschacht *et al.* (1988) and Auvergne *et al.* (1990). In the proposed analysis, only the extraction of the output of the nMOS network will be discussed.

Considering the two pass transistors of each network, up to 16 input combinations for the CPL NAND2 gate exist depending on whether a signal is considered as V_{DD}, GND, rising or falling ramp (figure 2). Each of these cases will be discussed next and it will be shown that the analysis of a CPL gate can be performed at a low level of complexity for every possible combination of input ramps.

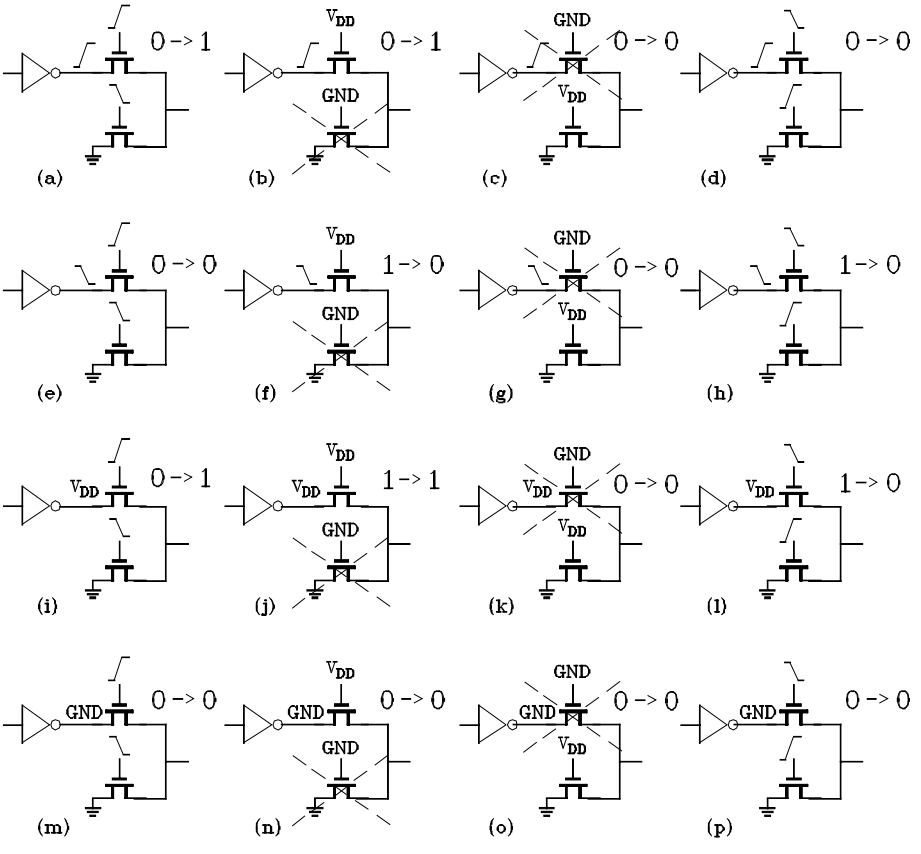


Figure 2. Input patterns for NAND2 CPL gate.

2.1. *Cases (a), (b), (i)*

For these cases one of the input signals, either the output of the driving inverter or the gate signal A, is transferred to the output. For cases (a) and (i) where a ramp input is applied to transistor gates, the pass transistor which is connected to ground acts as a short-circuiting device slowing down the output charging while in case (b) it has no effect since it is cut-off. The way in which the output waveform is obtained in these cases will be described in the next section.

2.2. *Cases (c), (g), (k), (o)*

For these cases only the transistor which has its source node connected to ground is conducting since the other pass transistor has a grounded gate signal. Consequently, independently of input B, no transition at the output node exists which remains tied to zero.

2.3. *Cases (d), (e), (m), (p)*

For the inputs of these cases no output transition occurs. A glitch on the output node may occur, however the estimation of the duration and value of such glitches is not within the goals of this work.

2.4. *Cases (j), (n)*

The conducting pass transistor in these two cases receives a steady V_{DD} gate signal and input B is also constant at V_{DD} and GND respectively. As a result, no output transition occurs and the output remains constant at its initial value.

2.5. *Cases (h), (l)*

In these cases the signal which is actually passed to the output is the GND signal since the pass transistor which is tied to ground receives as gate signal a rising ramp. The other pass transistor has an insignificant effect on the output waveform as will be explained in § 3 where the calculation of the output waveform will be discussed.

2.6. *Case (f)*

In this case, which will be described in § 3, the output of the driving inverter is a falling ramp which is passed to the output through a fully conducting pass transistor. The pass transistor, which is tied to ground is cut-off and consequently it does not affect the output waveform.

3. Output waveform evaluation

3.1. *Cases (a), (b), (i)*

In order to obtain the output waveform of the NAND2 gate a four-step process will be followed according to the distinct subcircuits that can be defined. This process is shown diagrammatically in figure 3 and offers the possibility of estimating the performance of a CPL gate in a simple and computationally inexpensive way. The first step of the analysis is to determine the output waveform of the structure consisting of an inverter driving a single pass transistor (signal O in figure 1(b)). The use

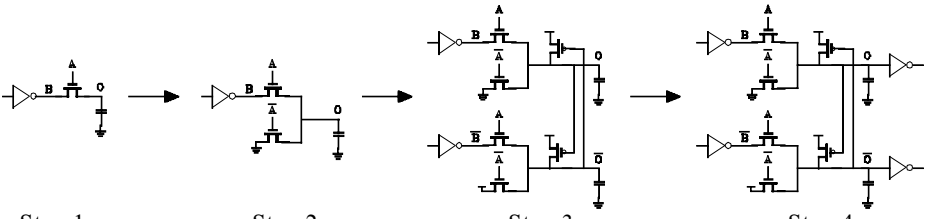


Figure 3. Four-step process for obtaining the output waveform of a NAND2 CPL gate.

of a single pass transistor in the output of an inverter is very common in CMOS design (e.g. latches). For the following, it should be noted that when the gate signal A of the pass transistor is V_{DD}, signal V_B is transferred to O with a small delay but the output waveform at O does not reach V_{DD} since close to $V_O \approx V_{DD} - V_T$ the pass transistor turns off

$$(V_T = V_{TN}|_{V_{SB} \approx V_{DD} - V_{TO}} = V_{TO} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})|_{V_{SB} \approx V_{DD} - V_{TO}}$$

where V_{TN} is the threshold voltage and V_{TO} is the zero bias threshold voltage of an nMOS transistor). It should also be mentioned that the alpha power law model proposed in Sakurai and Newton (1990) will be used for the transistor currents. For the case of an nMOS transistor the model is described by the

$$I_D = \begin{cases} 0 & V_{GS} \leq V_{TN}\text{: cutoff region} \\ k_l(V_{GS} - V_{TN})^{a/2} V_{DS} & V_{DS} < V_{DSAT}\text{: linear region} \\ k_s(V_{GS} - V_{TN})^a & V_{DS} \geq V_{DSAT}\text{: saturation region} \end{cases} \quad (1)$$

where V_{DSAT} is the drain saturation voltage, k_l, k_s are the transconductance parameters, α is the carrier velocity saturation index.

Step 1: Modelling pass transistor operation

In the case where ramp inputs are applied to the pass transistor terminals, the behaviour of the pass transistor is determined by the timing relation between these ramps. In order to confront the complexity of this problem two major cases are considered. The first case is when the gate input effectively acts as V_{DD} and the output voltage is determined by the drain input. The second case is when the gate input cannot be considered as V_{DD}, where it substantially determines the output voltage. These two cases can model all input combinations with sufficient accuracy.

Therefore, a comparison between the input waveforms V_A and V_B has to be made. V_B is obtained by performing transient analysis on the driving inverter having its output load increased by the capacitive load at the output of the nMOS network. Let t_g^s, t_{inv}^s and t_g^e, t_{inv}^e be the starting and ending time points of gate signal V_A and signal V_B respectively. We define the quantity $d = [(t_g^e - t_{inv}^e) + (t_g^s - t_{inv}^s)]/\tau_g$ where τ_g is the transition time of the gate signal. If $d < -0.5$ the gate signal should be considered as V_{DD}. Otherwise, signal V_A cannot be considered as V_{DD} compared to V_B and the output voltage follows the gate input. The above limit leads to sufficient accuracy especially in cases where there are no significant differences between the slopes of the input signals. From the above definition it becomes clear that case (a), where equal ramp inputs are employed, is treated as case (i).

(a) *V_A does not act as V_{DD}.* When V_A cannot be considered as V_{DD} compared to V_B, cases (a) and (i), the output waveform at point O follows the gate signal with a delay which is due to the fact that the source voltage of the pass transistor is always lower than the gate signal by V_{TN} and this difference is increasing as the source voltage increases because of the body effect. This is valid because nodes in CPL present low capacitance. Considering that the gate signal is $V_A = gt$ where g is its slope and that the threshold voltage can be approximated by a first order Taylor series around $(V_{DD} - V_{TO})/2$ as $V_{TN} = k_1 + k_2 V_{SB}$ the output waveform at point O is given by

$$V_{out} = V_g - V_{TN} = gt - k_1 - k_2 V_{out} \quad \Rightarrow \quad V_{out} = \frac{gt - k_1}{1 + k_2} \tag{2}$$

In order to validate the proposed approximation, output waveform comparisons between simulated and calculated results are shown for a 0.25 μm technology in figure 4, for several marginal cases ($d = -0.5$). In figure 5, calculated output waveform results for this step are compared to simulated ones for varying pass transistor widths for marginal cases ($d = -0.5$). As it can be observed, the output does not vary significantly with transistor width although the worst case is considered and the evaluation of the output by relating it to the gate signal provides sufficiently accurate results.

It should be mentioned, that for very fast gate inputs (e.g. when the transition time of the gate signal is lower than the transition time of a step response), the output voltage will not follow the gate signal according to equation (2). In that case and if higher accuracy is required, the differential equation that corresponds to the charging of the output capacitance through a transistor operating in saturation, can be solved considering a step input for the gate signal:

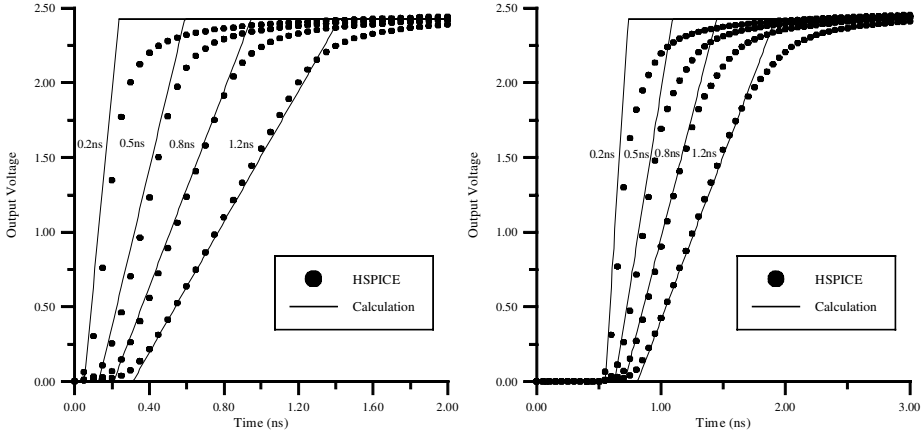


Figure 4. Simulated and calculated results for Step 1 of the proposed method for a TSMC 0.25 μm technology and two V_{in}, V_g combinations: (*a*) V_{in}, V_g starting at the same time point, (*b*) V_{in} starting 0.5 ns earlier than V_g. Transition time of V_{in} is selected so that $d = -0.5$ (limit case for the proposed method). Transition time for V_g is shown for each waveform.

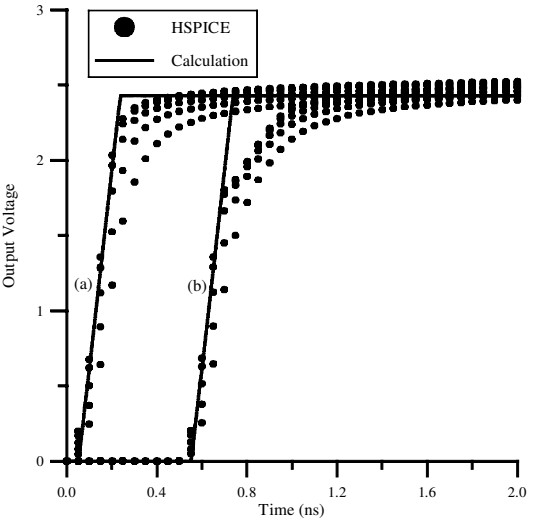


Figure 5. Simulated and calculated results (output waveforms of Step 1) for varying pass transistor widths (1, 2, 4, 8, 12 μm) for the two input patterns of figure 4 with $\tau_g = 0.2$ ns and $d = -0.5$ (worst case-output is calculated according to equation (2)) (TSMC 0.25 μm technology).

$$i_n(t) = C_L \frac{\mathrm{d}V_{out}}{\mathrm{d}t} \quad \Rightarrow \quad k_s(V_{DD} - V_{out} - V_T)^a = C_L \frac{\mathrm{d}V_{out}}{\mathrm{d}t} \tag{3}$$

Setting $a = 1$ (for a 0.25 μm technology $a = 1.14$) and $V_{out}[0] = 0$

$$V_{out} = (V_{DD} - V_T)\left[1 - \exp\left(-\frac{k_s t}{C_L}\right)\right] \tag{4}$$

Since the aim is to obtain a constant slope in order to model the output waveform by a ramp, the output can be approximated by its first order Taylor series at $t = 0.693(C_L/k_s)$, which is the time point at which the output reaches the 50% point.

(b) *V_A acts as V_{DD}.* In the case where V_A acts as V_{DD}, V_B is approximated by a linear function of time with slope s_{inv} and the network output waveform is obtained as a linear function of time with slope s_1 which has to be found. Waveform V_B can be approximated from the output waveform of the driving inverter with very good accuracy by a ramp which crosses the output waveform at $V_{DD}/2$ and has a slope equal to 70% of the slope of the actual waveform at $V_{DD}/2$ (Hedenstierna and Jeppson 1987). Moreover, the pass transistor can be considered as a resistance (figure 6) since it operates in the linear region. The value of the resistance can be calculated as $R = 1/[k_{l_n}(V_{GS} - V_{TN})^{a/2}]$ at $V_{GS} = (V_{DD} - V_T)/2$ and $V_{TN} \approx V_T$. According to this, the differential equation at node O becomes

$$i_n = C_L \frac{\mathrm{d}V_{out}}{\mathrm{d}t} \quad \Rightarrow \quad \frac{V_B - V_{out}}{R} = C_L \frac{\mathrm{d}V_{out}}{\mathrm{d}t} \quad \Rightarrow \quad RC_L \frac{\mathrm{d}V_{out}}{\mathrm{d}t} + V_{out} - s_{inv} t = 0 \tag{5}$$

which has the solution

$$V_{out} = s_{inv} t + RC_L s_{inv}(\mathrm{e}^{-t/RC_L} - 1) \tag{6}$$

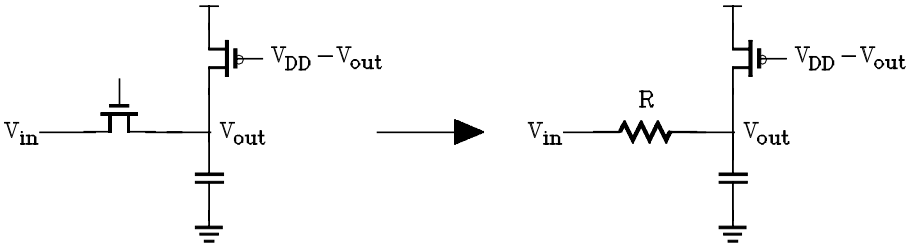


Figure 6. Handling of case (b) for NAND2 CPL.

under the initial condition $V_{out}[0] = 0$. In order to model the output waveform by a ramp, a slope for the output waveform can be obtained by solving differential equation (5) setting $V_{out} = s_1 t$ which leads to $s_1 = s_{inv} t/(RC_L + t)$. To determine an appropriate time point for the calculation of an average value for s_1, the following approach is considered. The output waveform for $t \to \infty$ is bounded by the line $b(t) = s_{inv} t - RC_L s_{inv}$. $b(t)$ reaches the maximum value for the output voltage $(V_{DD} - V_T)$ at $t_{th} = [(V_{DD} - V_T)/s_{inv}] + RC_L$. The output waveform, due to low capacitance values at CPL nodes will very quickly, after the application of the input, coincide with line $b(t)$. Consequently, slope s_1 can be calculated at $t_{th}/2$ leading to

$$s_1 = s_{inv} \frac{V_{DD} - V_T + RC_L s_{inv}}{V_{DD} - V_T + 3RC_L s_{inv}}$$

The accuracy of the techniques employed in Step 1 is demonstrated in figure 7, plot I for cases (i), (b) and (a) respectively. In these plots, the simulated and calculated output waveform of a single pass transistor which is driven by an inverter is shown, together with the signals that are applied at the pass transistor terminals, namely the output of the driving inverter and the gate signal. Results are plotted for two submicron technologies (HP 0.5 μm and TSMC 0.25 μm), for NAND2 CPL gates with the following configuration:

0.5 μm: $V_{DD} = 5$ V, Inverter: $W_n = 4$ μm, $W_p = 6$ μm, $L = 0.5$ μm, Pass transistors: $W_n = 6$ μm, Pull up trans.: $W_p = 4$ μm, $C = 50$ fF.
0.25 μm: $V_{DD} = 3.3$ V, Inverter: $W_n = 1.4$ μm, $W_p = 2.1$ μm, $L = 0.25$ μm, Pass transistors: $W_n = 2.1$ μm, Pull up trans.: $W_p = 1.4$ μm, $C = 30$ fF.

The main SPICE parameters for both technologies are given in table 1.

Step 2: Incorporation of short-circuit pass transistor effect

The next step is to consider the effect of the nMOS transistor, M_{gnd}, which has one terminal connected to ground (top subcircuit in figure 1(*a*)). In the case where the gate signal A is considered as V_{DD} compared to V_B, the gate signal $\bar{A}$ of transistor M_{gnd}, will effectively act as GND and the transistor will be cut-off without having any effect on the output waveform at point O (case (b)). In the case where the gate signal A cannot be considered as V_{DD} it is reasonable to assume that up to a time point, transistor M_{gnd} will be conducting, thus draining the capacitance charging current to ground. Consequently, up to this time point, t_s, which was found to be close to the time when the gate signals reach $V_{DD}/2$, the output voltage remains at its initial value. In other words it is considered that both pass transistors are

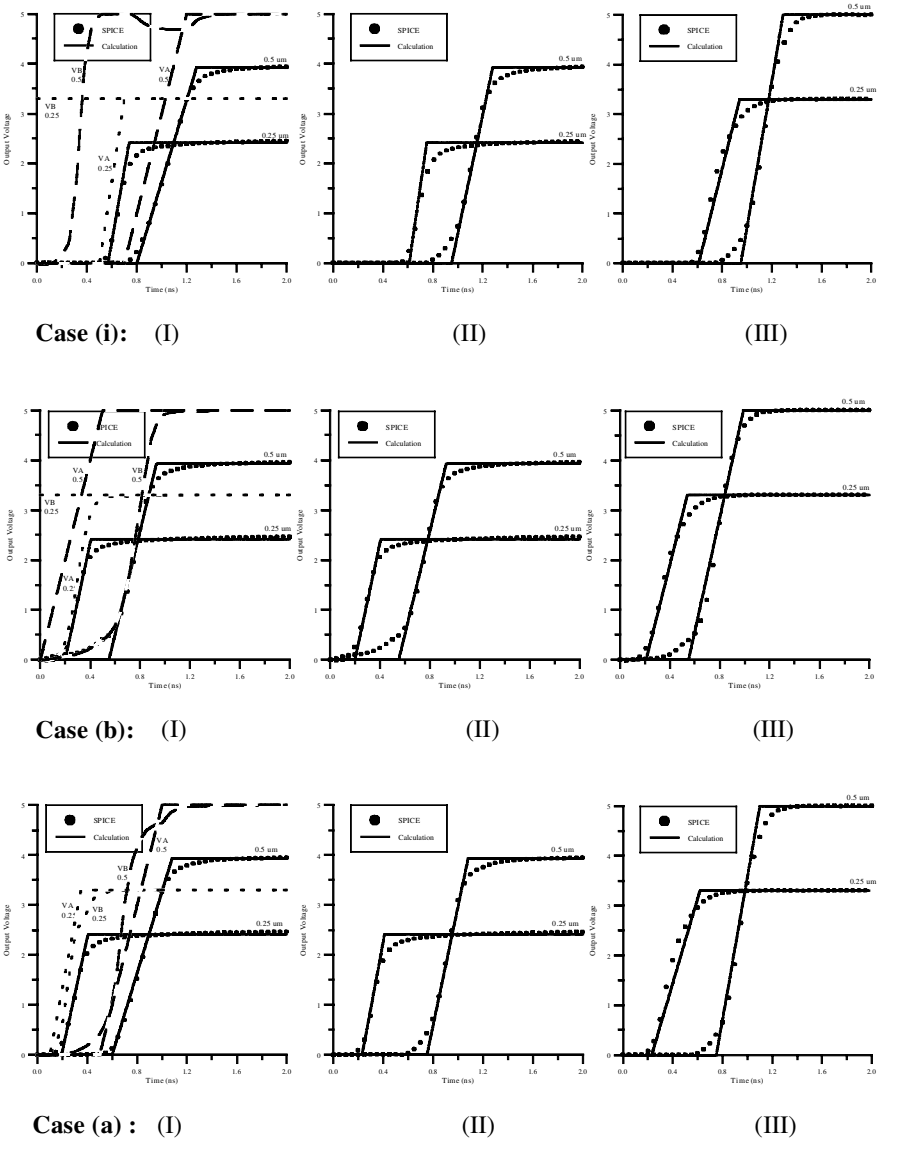


Figure 7. Output waveform comparison between simulated and calculated results for the three steps of the NAND gate output estimation. Case (i): 0.5 μm, $V_{in} = [0\,\text{ns}, 5, 0.5\,\text{ns}, 0]$ and $V_A = [0\,\text{ns}, 0, 0.7\,\text{ns}, 0, 1.2\,\text{ns}, 5]$; 0.25 μm, $V_{in} = \text{DC}\,0\,\text{V}$ and $V_A = [0\,\text{ns}, 0.5\,\text{ns}, 0, 0.7\,\text{ns}, 3.3]$. Case (b): 0.5 μm, $V_{in} = [0\,\text{ns}, 5, 1\,\text{ns}, 0]$ and $V_A = [0\,\text{ns}, 0, 0.5\,\text{ns}, 5]$; 0.25 μm, $V_{in} = [0\,\text{ns}, 3.3, 0.3\,\text{ns}, 0]$ and $V_A = \text{DC}\,3.3\,\text{V}$. Case (a): 0.5 μm, $V_{in} = [0\,\text{ns}, 5, 1\,\text{ns}, 0]$ and $V_A = [0\,\text{ns}, 0, 0.5\,\text{ns}, 0, 1\,\text{ns}, 5]$; 0.25 μm, $V_{in} = [0\,\text{ns}, 3.3, 0.3\,\text{ns}, 0]$ and $V_A = [0\,\text{ns}, 0, 0.1\,\text{ns}, 0, 0.35\,\text{ns}, 3.3]$. V_{in} is the input to the driving inverter.

charging/discharging the output load with the same current thus leading to a charge equilibrium in the output. Consequently the starting point of the output waveform, which was calculated in Step 1 (see table 2) has to be shifted to time point t_s. However, the ending time point of the output waveform remains unchanged resulting in a steeper increase of the output voltage.

Name	Comment	Units	HP 0.5 μm (Level = 3) nMOS	HP 0.5 μm (Level = 3) pMOS	TSMC 0.25 μm (Level = 49) nMOS	TSMC 0.25 μm (Level = 49) pMOS
U0	Mobility	$cm^2/(V s)$	546.2	135.5	455.3	158.6
VMAX	Maximum drift velocity	m/s	2.008×10^5	2.542×10^5	—	—
VSAT	Saturation velocity of carrier	m/s	—	—	1.050×10^5	1.850×10^5
TOX	Gate oxide thickness	m	9.6×10^{-9}	9.6×10^{-9}	5.8×10^{-9}	5.8×10^{-9}
VTO	Zero bias threshold voltage	V	0.6566	−0.9213	0.4308	−0.6158

Table 1. SPICE model parameters for two submicron technologies.

In plot II of figure 7, the simulated and calculated output waveform of a network of a CPL gate (excluding the pMOS restoring transistor) is shown for cases (i), (b), (a) respectively. As it can be observed, the effect of the short-circuiting transistor M_{gnd} is accurately captured by the proposed analysis for cases (a) and (i). The shift in time of the starting point of the waveforms in plot II compared to plot I respectively, can be readily observed.

Step 3: Incorporation of the pMOS transistor restoring effect

In this step, the effect of the pMOS restoring transistor on the output waveform at point O has to be taken into account. Since the gate of this transistor is driven by the output of the symmetrical network which in turn is approximately the symmetrical waveform of point O, assuming that waveform at point O is rising, $\bar{O}$ would be falling. Consequently, up to the time point when the pMOS transistor starts conducting strongly (the time when $\bar{O}$ reaches the 50% point) the output waveform at point O is that determined in step 2. From this point on, the pMOS transistor pulls the output voltage to V_{DD} contributing to a faster charging of the output capacitance. This increased charging rate can be captured accurately by increasing from this point on the slope of the output waveform. The slope of the output waveform after the pMOS transistor starts conducting can be calculated as follows:

(a) *V_A acts as V_{DD}.* Let us consider a single pass transistor driving an output load and a pMOS restoring transistor. Since the nMOS pass transistor operates in the linear region it can be considered as a resistance R whose value was calculated in the previous §(figure 6). In order to enable the mathematical analysis the input waveform is approximated by a ramp with slope s_{inv} and the output waveform by a ramp with slope s_3. Since the gate of the pMOS restoring transistor in a CPL gate is driven by the output of the symmetrical network, it can be assumed that $|V_{GS}| = |V_{DD} - V_{out} - V_{DD}| = |-V_{out}|$. Considering that the pMOS restoring transistor operates in the linear region, the differential equation at the output node can be written as

$$i_n + i_p = C_L \frac{dV_{out}}{dt} \quad \Rightarrow \quad \frac{s_{inv}t - s_3 t}{R} + k_{l_p}(s_3 t - V_{TP})^{a_p/2}(V_{DD} - s_3 t) = C_L s_3 \qquad (7)$$

From the above equation the slope of the output waveform can be calculated as a function of time. It has been found that calculating the output waveform at $\frac{3}{4}\tau_2$ where τ_2 is the transition time of the output waveform at Step 2, gives sufficiently accurate results. (In order to solve the above equation for s_3, s_3 is set equal to s_2 in

(a)	(b)	(c)	(d)
$t_s = t_g + \frac{V_{DD}}{2g}$ $s_1 = \frac{g}{1+k_2}$ $s_2 = \frac{2g(V_{DD}-V_T)}{V_{DD}(1+2k_2)-2V_T(1+k_2)+k_1}$ $s_{out} = \frac{2s_2s_3}{s_2+s_3}$	$t_s = t_{inv}$ $s_1 = s_{inv}\frac{V_{DD}-V_T+RC_Ls_{inv}}{V_{DD}-V_T+3RC_Ls_{inv}}$ $s_{out} = \frac{2s_1s_3}{s_1+s_3}$	No transition	No transition
(e)	(f)	(g)	(h)
No transition	$t_s = t_{inv} + \frac{V_T}{s_{inv}}$ $s_{out} = \frac{V_{DD}s_{inv}}{V_{DD}-V_T}$	No transition	$t_s = t_{50\%} - \frac{V_{DD}}{2s_{out}}$ s_{out} from inverter analysis
(i)	(j)	(k)	(l)
$t_s = t_g + \frac{V_{DD}}{2g}$ $s_1 = \frac{g}{1+k_2}$ $s_2 = \frac{2g(V_{DD}-V_T)}{V_{DD}(1+2k_2)-2V_T(1+k_2)+k_1}$ $s_{out} = \frac{2s_2s_3}{s_2+s_3}$	No transition	No transition	$t_s = t_{50\%} - \frac{V_{DD}}{2s_{out}}$ s_{out} from inverter analysis
(m)	(n)	(o)	(p)
No transition	No transition	No transition	No transition

Table 2. Network output waveform slopes for CPL NAND2 gate.

the term that is powered to $a_p/2$). According to this, once the output waveform at Step 2 is obtained, the slope of the output waveform after the time when the output voltage reaches $V_{DD}/2$ should be increased to s_3.

(b) *V_A does not act as V_{DD}.* In this case, the gate-to-source voltage V_{GS} of the pass-transistor is small since the output voltage 'follows' the gate signal. Consequently the current through the pass transistor is extremely small and at the time when the pMOS transistor starts strongly conducting the output node voltage is determined only by the current of the pull-up pMOS device. According to this, the output waveform slope increase after the time when the output waveform according to Step 2 reaches $V_{DD}/2$, is independent of the drivability of the nMOS pass transistor. The increased slope can be obtained by solving the differential equation at the output node considering the output voltage as a ramp

$$i_p = C_L \frac{\mathrm{d}V_{out}}{\mathrm{d}t} \quad \Rightarrow \quad k_{l_p}(s_3 t - V_{TP})^{a_p/2}(V_{DD} - s_3 t) = C_L s_3 \tag{8}$$

s_3 is calculated at $t = \frac{3}{4}\tau_2$. The slope of the output waveform obtained in Step 2 should be increased to s_3 after the time the output voltage crosses $V_{DD}/2$.

Since the starting and ending point of the waveform at point O are known, the ramp that represents the output waveform of the complete CPL network can be defined by connecting these two points, resulting in the final slope, s_{out}.

In figure 7, plot III, simulated and calculated results are shown for a complete network including the restoring pMOS transistor for cases (i), (b) and (a) respectively. Consequently, these results correspond to the application of the proposed technique at all three steps. It can be observed that the proposed method is accurate for each of the presented steps as well as for the overall output response.

In table 2 the slope of the network output waveform of the CPL gate (the output is represented as a ramp signal) together with the starting point of the output evolution is presented for each case. t_g is the starting point of the gate input signal. t_{inv} is the starting point of the ramp which corresponds to signal V_B.

Step 4 Obtaining the gate output waveform

As already mentioned the gate output waveform can be obtained by performing a transient analysis on the output inverter using analytical or macromodelling techniques and using the network output waveform that has been obtained from the previous steps as input to the inverter.

3.2. *Cases (h), (l)*

In the circuits which correspond to these cases the transistor which has its source node tied to ground is becoming increasingly conducting since it receives a rising input ramp as a gate signal. The other pass transistor is poorly conducting because its V_{GS} is throughout the output evolution close to zero. Consequently, the pass transistor node which is driven by the inverter of the preceding stage does not have any significant effect on the output waveform.

According to this, the output waveform can be obtained by solving the differential equation describing the discharging of a capacitance (initially charged at V_{DD}) through an nMOS transistor, which operates initially in saturation and then in the linear region. This is similar to the first approach in solving the differential equation

of an inverter for a rising input, when the effect of the pMOS transistor is neglected, which has been described in Hedenstierna and Jeppson (1987).

In order to capture the effect of the pMOS restoring transistor (Step 3) which pulls the output voltage up, it is considered that the pMOS current acts as an additional charge at the output node which has to be discharged to ground slowing down the output discharging. A rough estimation of this additional charge can be performed as follows. In this structure the maximum value of the pMOS current, which acts as a short-circuit current, occurs around the point when both its V_{GS} and V_{DS} are at the half V_{DD} point. Consequently, the maximum value, I_{pmax}, is calculated by setting in the current expression for the linear region $V_{GS} = V_{DS} = V_{DD}/2$,

$$I_{pmax} = k_{l_p}\left(\frac{V_{DD}}{2} - V_{TP}\right)^{a_p/2}\frac{V_{DD}}{2}$$

where V_{TP} is the threshold voltage of the pMOS transistor. The current is almost symmetrical around this point which is close to time point t_{s_p} where the pMOS transistor enters saturation and it can be represented by a piece-wise linear function (Hirata *et al.* 1996, 1998). Assuming for simplicity that the output evolution lasts as much as the gate signal transition, the additional charge can be approximated as

$$Q_{ad} = I_{pmax}\frac{(V_{DD} - V_{TP})\tau}{2V_{DD}} \tag{9}$$

where τ is the transition time of the gate signal.

Since the initially stored charge at the output node capacitance is $Q_{init} = C_L V_{DD}$, the additional charge can be considered as an increase of the output node capacitance by

$$C_{ad} = \frac{Q_{ad}}{V_{DD}} \tag{10}$$

If this capacitance is added to C_L and the output waveform is calculated, the output waveform matches that of the actual CPL network with very good accuracy. In figure 8 the calculated output waveform of a network whose conditions correspond to that of case (l) is shown (case (h) has exactly the same response) together with the response simulated by SPICE.

In table 2 and for cases (h), (l), it is considered that the output waveform is approximated by a ramp whose slope s_{out} is equal to 70% of the slope of the original waveform (taking into account the additional capacitive load of equation (10)) at the time point ($t_{50\%}$) when the output crosses $V_{DD}/2$.

3.3. *Case (f)*

For this case the pass transistor which has its source node connected to ground is cut-off. The output load will be discharged through the other pass transistor and the pMOS restoring transistor has the same effect as in the previously described cases (h), (l) and thus can be captured by an increased output node capacitance according to the average charge that the pMOS transistor contributed. This increased capacitance is taken into account when calculating the output waveform of the driving inverter. Finally, in order to obtain the output waveform at point O, since the pass transistor starts conducting when the input voltage at the source node drops to $V_{DD} - V_T$, at this time point the output should start being discharged. The ending

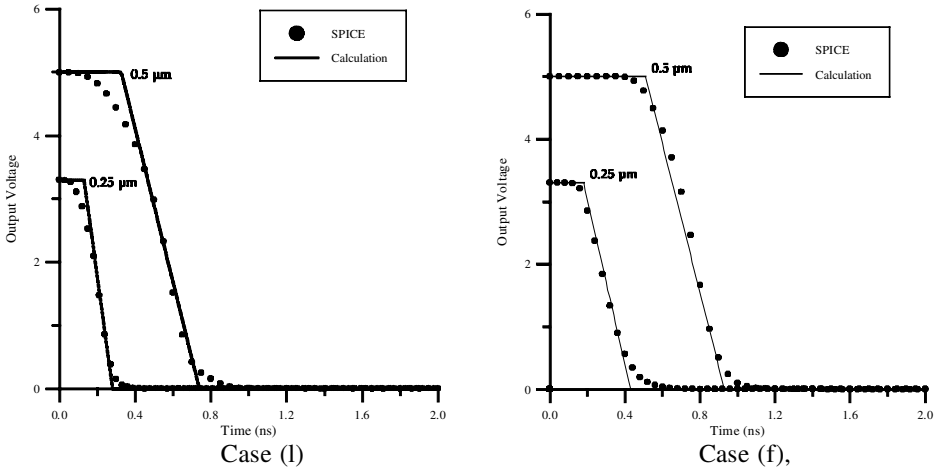


Figure 8. Output waveform comparison between simulated and calculated results for cases (l) and (f) of figure 2, for two submicron technologies. Case (l): 0.5 μm, $V_{\bar{A}} = [0\,\text{ns}, 0, 1\,\text{ns}, 5]$; 0.25 μm, $V_{\bar{A}} = [0\,\text{ns}, 0, 0.25\,\text{ns}, 3.3]$; Case (f): 0.5 μm, $V_{in} = [0\,\text{ns}, 0, 1\,\text{ns}, 5]$; 0.25 μm, $V_{in} = [0\,\text{ns}, 0, 0.25\,\text{ns}, 3.3]$.

time point (for example the time point when the output reaches $0.05V_{DD}$) remains unchanged. In this way a slope for the output waveform can be obtained that captures the actual output waveform at point O with sufficient accuracy. In figure 8 the calculated output response of a NAND2 CPL network whose operating conditions correspond to that of case (f) is shown together with the simulated response using SPICE.

In table 2 and case (f) the starting point and slope of the ramp that corresponds to the output waveform at point O is given and it is considered that the waveform at the output of the driving inverter, taking into account the additional capacitance C_{ad}, is represented by a ramp of the form $V_{inv} = V_{DD} - s_{inv}t$, starting at point t_{inv}.

3.4. *Synopsis*

In the previous paragraphs the treatment of the network, which includes a pass transistor tied to ground has been considered. The network of the NAND gate, which includes a pass transistor connected to V_{DD} can be studied in exactly the same way, since all possible input patterns correspond to the already presented cases in figure 2.

It should be noted that for each case the output waveform can be obtained not by traversing all steps that have been presented but by referring to a look up table (e.g. table 2), where the formula for the output waveform for each case has been stored. Since each case has been solved and the resulting slope and starting point have been precalculated, the output waveform of a CPL gate can be calculated efficiently. According to this simulation approach the speed cost is shifted from the transient analysis of each gate to the algorithm that detects and identifies each CPL gate and the case to which it corresponds according to the linearized inputs of the preceding stages, which are known before the transient analysis begins.

In order to illustrate the speedup that can be obtained by the application of the proposed methodology, execution times for HSPICE are compared to the

Case	V_{in}	V_A	Exec. Time (HSPICE) (s)	Exec. Time (Proposed) (s)	Speedup
(a)	pwl(0 ns, 3.3, 0.3 ns, 0)	pwl(0 ns, 0, 0.1 ns, 0, 0.35 ns, 3.3)	0.49	0.0235	20.85
(b)	pwl(0 ns, 3.3, 0.7 ns, 0)	pwl(0 ns, 0, 0.2 ns, 3.3)	0.39	0.0228	17.11
(h)	pwl(0 ns, 0, 0.4 ns, 0, 1 ns, 3.3)	pwl(0 ns, 3.3, 0.5 ns, 3.3, 1 ns, 0)	0.50	0.0241	20.75
(i)	DC 0	pwl(0 ns, 0, 0.5 ns, 0, 0.7 ns, 3.3)	0.55	0.0221	24.89
(l)	DC 0	pwl(0 ns, 3.3, 0.5 ns, 3.3, 1 ns, 0)	0.60	0.0215	27.91

Table 3. Speed comparison between HSPICE and the proposed method.

corresponding times for the proposed method implemented in *C*, in table 3. The presented cases correspond to a NAND2 CPL gate (including the two driving inverters), for a TSMC 0.25 μm technology with the following configuration: $V_{DD} = 3.3$ V, Inverter: $W_n = 1.4$ μm, $W_p = 2.1$ μm, $L = 0.25$ μm, Pass transistors: $W_n = 2.1$ μm, Pull up trans.: $W_p = 1.4$ μm, $C = 30$ fF, TRAN 0.01 ns, 2 ns. It should be mentioned that the observed speedup between SPICE and the proposed method, increases as the number of transistors in the simulated circuit increase.

The proposed methodology can be extended in order to cover transmission gate based logic styles: for the case of an inverter driving a transmission gate simulation results have shown that exactly the same technique can be employed, i.e. two main cases for the pair of gate signals (acting as $V_{DD}/0$ V or not) should be considered. However, in case the output follows the gate signal, there is no threshold drop and the output reaches the supply voltage.

4. Collapsing serial and parallel pass transistor structures

In the previous sections only a NAND CPL gate with two inputs has been considered. In other words each pass transistor structure under study received only one gate signal (e.g. signal A). In case of multiple input NAND/NOR CPL gates, the applied gate signals can be more than one, as for example in the AND4 gate shown in figure 9.

In the case where the subcircuit that has to be modelled consists of a string of serially connected transistors, it is obvious that the output node will start being charged/discharged when all transistors start conducting. The transistors are merged to form a single equivalent transistor (e.g. for equal transistor widths the width of the equivalent transistor is equal to the width of one transistor divided by the number of transistors). Consequently, the output voltage will either 'follow' the last gate signal or the transistor chain will be considered as a resistance. To define the last gate signal all gate signals which are in transition are taken into account. Finally, the effective gate signal is given by a ramp which starts at the last starting point of all gate signals and ends at the last ending point of all signals. Once the gate signal is determined, the output waveform of the gate can be found by applying the methodology that has been developed for the cases of a NAND2 gate.

The application of the above method, i.e. the extraction of the effective gate signal together with all other steps required in order to obtain the output waveform of an AND4 CPL network is examined in figure 10. The output waveform of the complete gate at point *O* as obtained by SPICE is compared to the output waveform which is calculated by the application of the above methodology, for three different

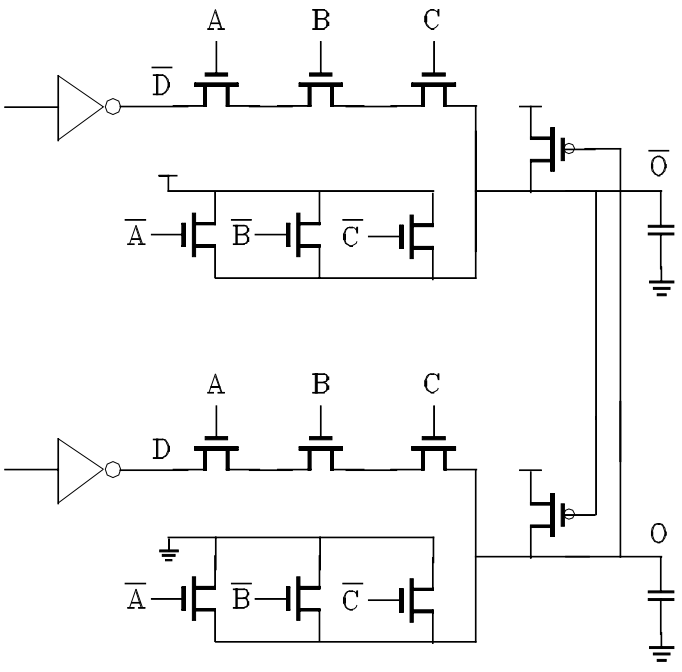
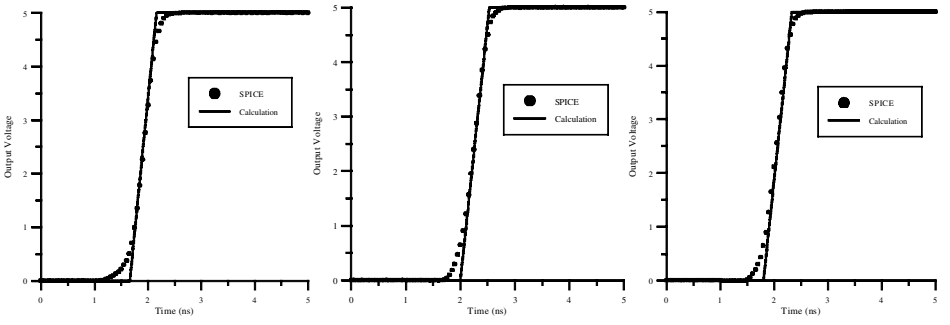


Figure 9. AND4 CPL gate (the output inverters have been omitted).



(*a*) (*b*) (*c*)

Figure 10. Output waveform comparison between simulated and calculated results for an AND4 CPL gate (all pass transistors $W_n = 6\,\mu m$, input inverter trans. $W_n = 6\,\mu m$, $W_p = 4\,\mu m$, restoring trans. $W_p = 4\,\mu m$, $L = 0.5\,\mu m$). (*a*) Three equal inputs $V_{g1} = [0\,ns, 0, 1\,ns, 0, 2\,ns, 5]$, $V_{g2} = [0\,ns, 0, 1\,ns, 0, 2\,ns, 5]$, $V_{g3} = [0\,ns, 0, 1\,ns, 0, 2\,ns, 5]$. (*b*) Three distinct inputs $V_{g1} = [0\,ns, 0, 1\,ns, 0, 2\,ns, 5]$, $V_{g2} = [0\,ns, 0, 1.2\,ns, 0, 2.2\,ns, 5]$, $V_{g3} = [0\,ns, 0, 1.6\,ns, 0, 2.4\,ns, 5]$. (c) Three crossing inputs $V_{g1} = [0\,ns, 0, 1\,ns, 0, 2\,ns, 5]$, $V_{g2} = [0\,ns, 0, 1.2\,ns, 0, 2.2\,ns, 5]$, $V_{g3} = [0\,ns, 0, 1.4\,ns, 0, 2\,ns, 5]$.

input patterns. The results prove the accuracy both of the gate input selection method as well as that of all other steps.

In the case where the subcircuit that has to be studied consists of parallel transistors the application of the algorithm presented in Jun *et al.* (1989) in order to extract a single equivalent signal for a group of parallel transistors has been found to

give sufficiently accurate results. It should be noted that the gate signal is determined on the conducting part of the network and the same signal is applied to the short-circuiting part.

5. Other pass transistor structures

5.1. *XOR gates*

In § 3 the example of a two input CPL NAND gate has been presented because it essentially allows the study of all possible input combinations to a CPL gate. For example let us consider the case of a XOR CPL gate (Zimmermann and Fichtner 1997) for which all possible input patterns are shown in figure 11. It will be shown that each case can be diminished to an equivalent case of the NAND2 CPL gate.

The last two rows of the matrix (cases (i)–(l) and (m)–(p)) correspond directly to a NAND2 CPL gate since the source node of one pass transistor is always tied to ground. The input combinations for cases (a) and (h) as well as cases (d) and (e) do not lead to a transition at the output node. The cases for which a transition on the output occurs, i.e. cases (b), (g) ($0 \rightarrow 1$) and (c), (f) ($1 \rightarrow 0$) can be analysed according to what has already been described for the NAND2 CPL gate since one of the pass transistors is cut-off because of a grounded gate node.

5.2. *MUX structures*

Multiplexer structures are used for certain types of logic functions; for example they are used extensively in the LEAP scheme that is proposed in Yano *et al.* (1996).

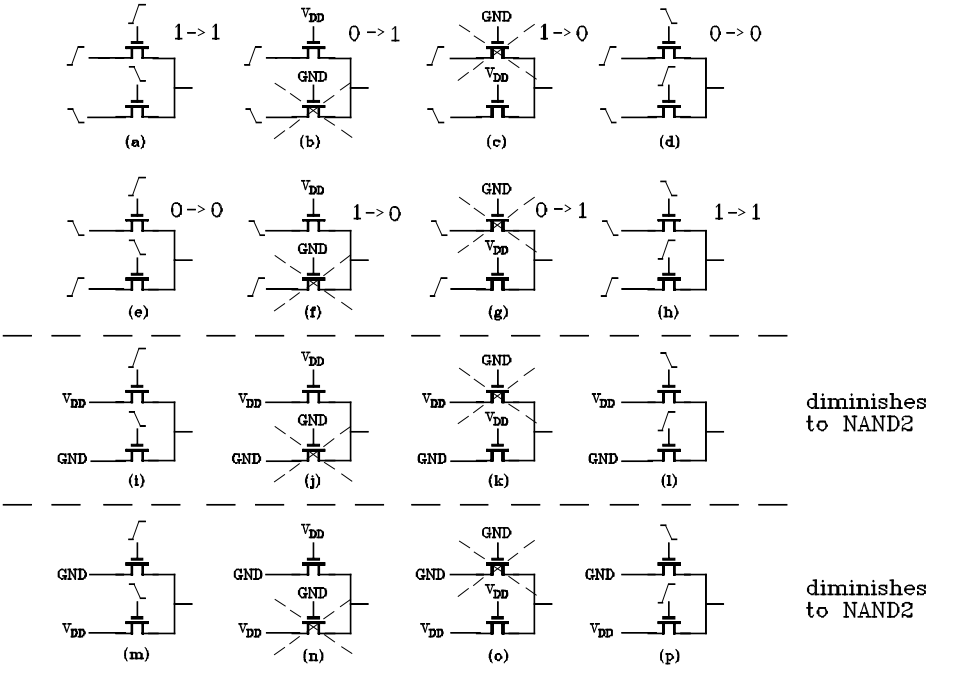


Figure 11. Input patterns for CPL XOR gate.

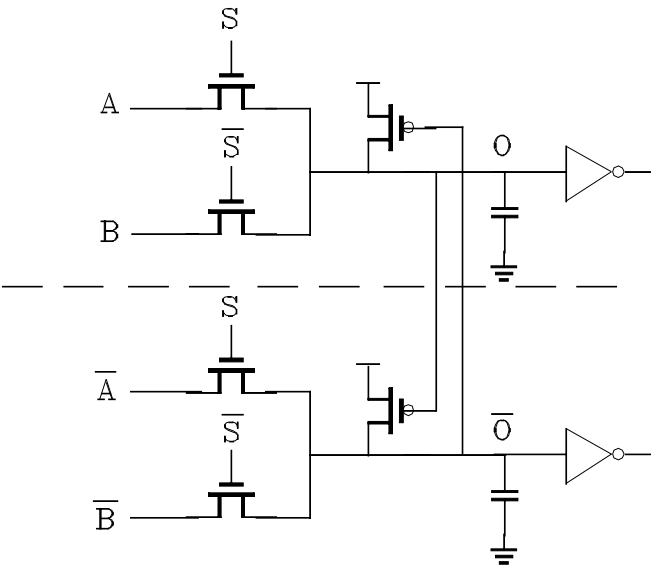


Figure 12. MUX2 structure in CPL.

A typical CPL MUX2 structure is shown in figure 12 where again each network can be studied independently.

Assuming that input signals A and B are either rising/falling ramps or V_{DD}/GND the following observations can be made. If one of the signals A, B is V_{DD} or G_{ND} the structure collapses to a NAND gate and can be modelled according to the methods described in § 3. If one of the select signals S, $\bar{S}$ is GND, the corresponding pass transistor is cut-off and the analysis of the remaining pass transistor can be performed as described earlier. The remaining cases are shown in figure 13. Cases (e), (f), (g), (h) will not be modelled as no transition at the output node occurs. For cases (a), (b) (which are the same), the pass transistor which receives a falling ramp as gate

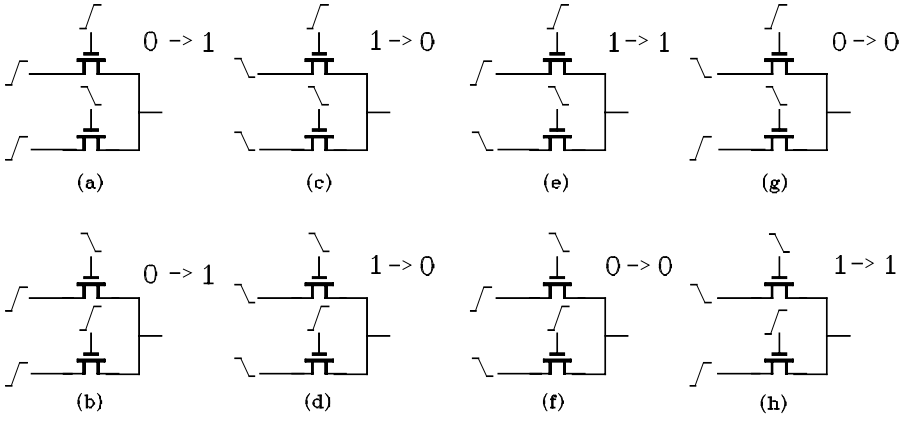
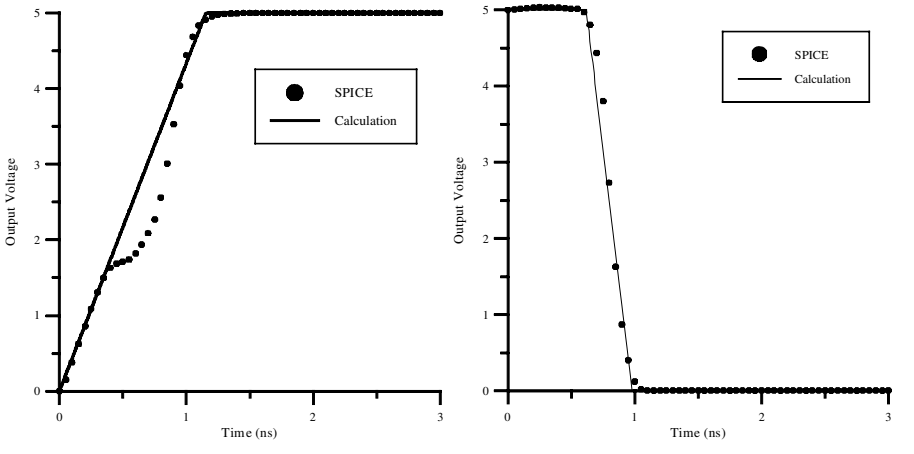


Figure 13. Input cases for a MUX structure.

signal, since its V_{GS} is initially high, will start passing the signal at its drain node to the output with a decreased slope (the transistor acts as a resistance R). This will continue up to the point where the gate signal falls to a low value (i.e. $V_{DD}/2$). From this point on, the pass transistor which receives the complementary rising gate signal will pass the signal applied at its drain node to the output. The output signal will reach V_{DD}-V_T at the time when the gate signal reaches V_{DD}. Consequently, the output signal is captured by a ramp which starts at the time when signal S starts and reaches V_{DD}-V_T at the time when signal S finishes its transition. The effect of the pMOS restoring transistor can be captured again by increasing the slope after the 50% point. The calculated and simulated output response of a MUX structure for this input pattern is shown in figure 14.

For cases (c), (d) (which are the same), the output node will start being discharged when the gate signal (e.g. signal S in case (c)) exceeds the drain/source input signal (e.g. signal A in case (c)) by V_T so that the pass-transistor starts conducting. From this point on the discharging current will increase rapidly (since drain and gate voltages have opposite slopes). For example, in case (c) the output waveform is captured by a ramp which starts when $V_S = V_A + V_T$ and ends when signal A falls to low values ($V_A = 0.05V_{DD}$). In figure 14 the calculated and simulated output response of a multiplexer corresponding to this case is shown.

Most of the CPL circuits are built in a regular form, i.e. the output of a CPL network is connected to the input of the next stage network and consequently the estimation of the output waveform can proceed gradually. According to the initial conditions at the gates of all pass transistors, the output load of the driving inverter is estimated. The driving inverter 'sees' as load all drain/source node capacitances up to the first pass transistor which is cut-off. If all pass transistors are initially conducting, all drain/source capacitances on the path to the output inverter, including its gate capacitance, are taken into account. The waveform at the output of the driving inverter is obtained using this load. Then, the output waveform of the first



Cases (a), (b) Cases (c), (d)

Figure 14. Output waveform comparison between simulated and calculated results for specific input patterns of the MUX2 structure (all pass transistors $W_n = 6\,\mu m$, restoring transistors $W_p = 4\,\mu m$, $L = 0.5\,\mu m$).

stage is obtained and is further propagated (depending on the gate signals of the pass transistors) in order for the next node voltage to be estimated. Gradually, the output waveform is obtained when all gate signals allow the input to propagate through the entire network.

In figure 15 a MUX4 implemented in CPL is shown. The previously described method can be applied to the subcircuits of this multiplexer as well. A comparison between the simulated and calculated waveform at the intermediate node I and the output node O is given in figure 16. For the input pattern shown in figure 16, in order to calculate the waveform at point I, case (a) of the NAND2 gate is employed without having to restore the output voltage to V_{DD} while for the calculation of the output waveform case (b) of the NAND2 gate is used.

5.3. *Application to the full adder*

The previously described methods for the modelling of pass transistor structures can be employed for estimating the output of more complex structures such as the full adder which consists of a gate producing the sum (figure 17) and a gate that generates the carry signal for the next stage. A full adder is a circuit block that is often implemented in CPL since it makes use of the advantages of this family (Zimmermann and Fichtner 1997). Such circuits, although complex at a first glance

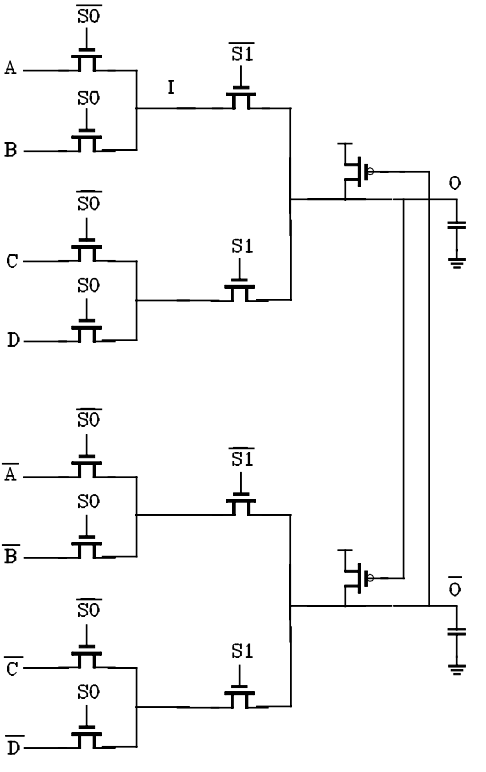
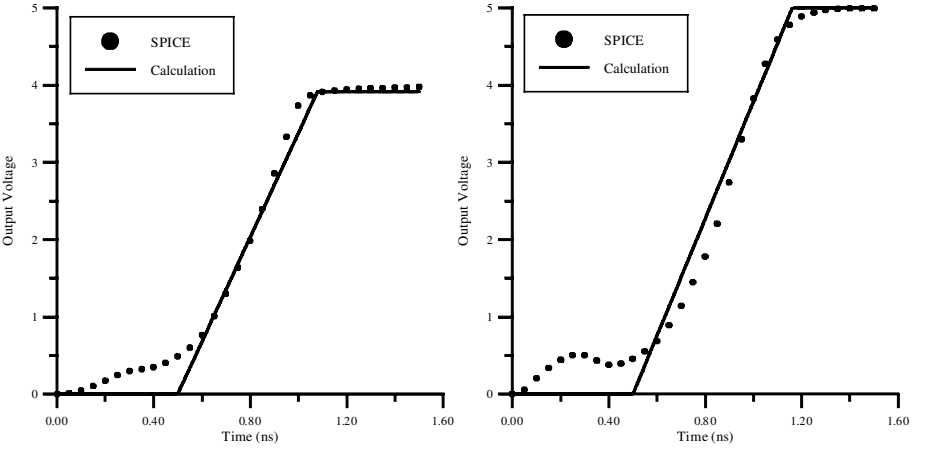


Figure 15. MUX4 (CPL).



(*a*) MUX4 I node (*b*) MUX4 0 node

Figure 16. Simulated and calculated results for the voltage waveform at the intermediate node (I) and the output node (O) of the MUX4 (all pass transistors $W_n = 6\,\mu m$, restoring transistors $W_p = 4\,\mu m$, $L = 0.5\,\mu m$). V_A: 0 V, V_B: [0 ns, 0, 1 ns,5], V_C: [0 ns, 0, 1 ns, 5], V_D: [0 ns, 5, 1 ns,0], V_{S0}: [0 ns, 0, 1 ns, 5], V_{S1}: [0 ns, 5, 0.5 ns,0].

can be analysed using the developed methodologies for NAND, XOR and MUX structures.

Let us consider the sum circuit when the patterns that are shown are applied. The analysis can proceed by first obtaining the output waveform of the first stage (i.e. at point I of the top subcircuit) and then that of the second stage. For the applied pattern the waveform at intermediate point I is obtained considering the NAND2 case (i) without restoring the output voltage to V_{DD}. A comparison between the calculated and simulated waveform using SPICE for this point is shown in figure 18(*a*). Having the waveform at point I the output SUM can be obtained as in case (b) of the NAND2 gate since the pass transistor that receives signal CI is cut-off. Here the pMOS pull-up transistor restores the output voltage level back to V_{DD}. A comparison of the calculated and simulated output waveform for the SUM is shown in figure 18(*b*). The circuit that generates the carry signal can be modelled in a similar way.

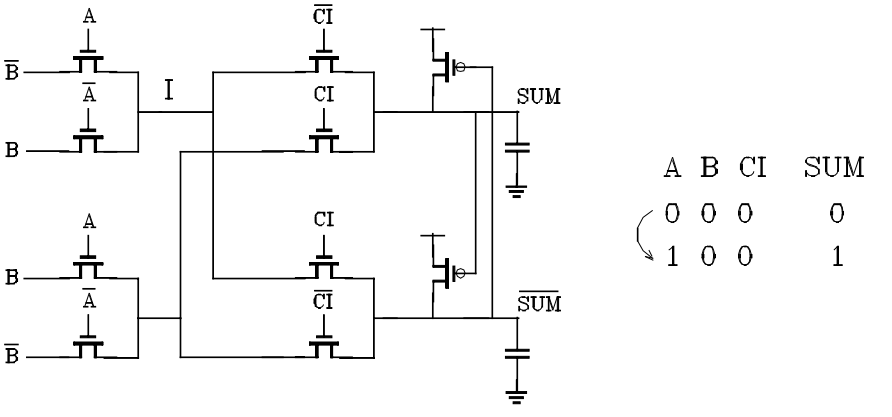
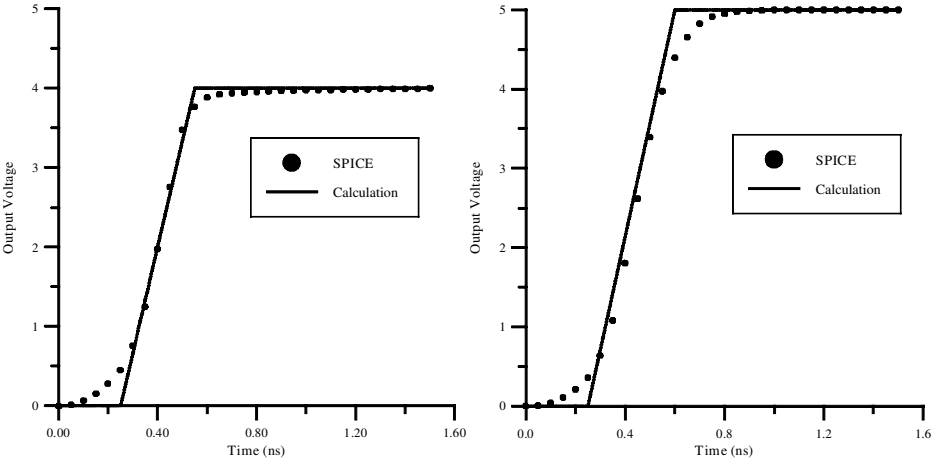


Figure 17. Sum circuit of the full adder.



(*a*) Waveform at the intermediate node (*b*) Waveform at the output(sum)

Figure 18. Simulated and calculated results for the voltage waveforms at the intermediate (I) and the output node for the SUM circuit when the following transition occurs: ABC 000 $\rightarrow$ 100 (thus SUM 0 $\rightarrow$ 1) (all pass transistors $W_n = 6\,\mu m$, restoring transistors $W_p = 4\,\mu m$, $L = 0.5\,\mu m$).

It is obvious that by simple manipulations, the output waveform of every pass transistor logic structure can be obtained with very good accuracy compared to SPICE simulations. Moreover, the output voltage extraction is performed at low computational cost since no complicated mathematical formulas are used, allowing the development of fast timing simulators.

6. Conclusions

An efficient and accurate methodology for modelling logic styles that employ pass transistor structures has been introduced. It is shown that a NAND2 CPL gate can be analysed by partitioning a circuit according to the distinct sub-circuits that coexist. The output waveform extraction involves only a few simple mathematical operations enabling the analysis of pass-transistor structures at fast times. The developed techniques are extended to other structures such as XOR gates and multiplexers while every circuit implemented in pass-transistor logic can be modelled. The significance of the proposed methodology lies mainly on the fact that although analytical or macromodelling techniques for conventional CMOS logic have matured, no efficient modelling techniques have been developed for pass-transistor logic. It is hoped that the presented approach will trigger further research on the field of modelling PTL/CPL circuits so that fast and accurate timing simulators for design automation tools can be developed.

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