0.92 for circuit B, and 157 kHz and 2.09 for circuit C, respectively. Fig. 4(a) shows the responses for the highpass and lowpass functions of the three-input single-output filter. Its bandpass responses are shown in Fig. 4(b). All the results are in good agreement with the theoretical predictions.

In the same way, the responses for the HSPICE simulation of the single-input three-output universal filter in Fig. 1 are shown in Fig. 5, when it functions as highpass and lowpass modes. The simulated results for the CCII±-based single-input three-output universal filter of Fig. 2 are shown in Fig. 6. The simulated f_o and Q are 159 kHz and 0.55 for circuit A, 159 kHz and 0.99 for circuit B, and 159 kHz and 1.77 for circuit C, respectively. As shown, the results also confirm the theoretical ones.

As indicated in the previously published paper [22], the parasitic impedances of nonideal current conveyors also affect the frequency performance of the circuits. In this case, larger values of C_1 and G_2 and lower values of G_1 and C_2 in Figs. 1 and 2 will contribute to the reduced loading effects, that agrees with our simulation results. Thus, the filters behave better for low-Q applications and the useful frequency range mainly relies on the bandwidths of the current and voltage transfers of current conveyors [22]. To improve the deviation to theoretical responses, high-performance CCII± and CCIII± with minor parasitic effects must be employed.

V. Conclusion

A versatile multi-input multi-output current-mode biquad configuration is introduced first in this brief. Its versatility has been exhibited by application on the implementation of three-input single-output and single-input three-output universal filters. In addition, by slight modification of the proposed scheme, another more useful single-input three-output construction has been obtained. Only three current conveyors and four grounded passive elements are necessary in both proposed filters. Many advantaged textures have been demonstrated. The simulation results confirm the theoretical analysis and a discussion of means to improve the responses is also included.

Acknowledgment

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Modeling CMOS Gates Driving RC Interconnect Loads

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***Abstract*—The problem of estimating the performance of CMOS gates driving RC interconnect loads is addressed in this paper. The widely accepted π-model is used for the representation of an interconnect line that is driven by an inverter. The output waveform and the propagation delay of the inverter are analytically calculated taking into account the coupling capacitance between input and output and the effect of the short-circuit current. In addition, short-circuit power dissipation is accurately estimated. Once the voltage waveform at both the beginning and the end of an interconnect line are obtained, a simple method is employed in order to calculate the voltage waveform at each point of the line.**

***Index Terms*—Modeling, propagation delay, short-circuit power.**

I. Introduction

With continuously decreasing device dimensions, the effect of the interconnect lines on the overall performance of digital integrated cir-

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cuits is becoming increasingly significant. As it has been extensively pointed out [1], [2], when the resistive component of the interconnect load becomes comparable to the gate output impedance, a single capacitor is no longer a valid gate load model. The line resistance R acts as capacitance "shielding," and as it increases this "shielding" becomes significant and the output waveform presents an RC tail. This is even more intense in submicrometer circuits where interconnect lines are longer and their distributed resistance larger. Therefore, more accurate load models have to be used for taking into account the increased role of the resistance in the determination of the load behavior and consequently the propagation delay of the driving CMOS gates.

Much research effort has been devoted during the last few years to modeling CMOS gates driving simple capacitive loads [3]–[5]. Expressions for the propagation delay of CMOS gates driving RC loads have also been derived [6]–[8], but they present significantly lower accuracy mainly because they are based on simplified assumptions for the transistor operation and use simple load models for the representation of the interconnect lines.

In order to find analytical expressions for the propagation delay and the output waveform shape, an interconnect line may be modeled in different ways [1]. An expression for the propagation delay when a load is modeled simply by a resistor in series with a capacitor was derived in [6]. However, the driving transistor was considered to operate always in linear mode and only the simplified case of step input was examined. In [7], the RC output load was replaced by an "effective" capacitance, which was calculated by an iteration procedure based on simplified assumptions for the shape of the output response. The real output waveform was approximated by the charging/discharging of the effective capacitance up to a point and capturing of the remaining portion of the output response is achieved by a simple resistive model. Another approach was proposed in [8] where a time-varying Thevenin equivalent model is used for the estimation of the gate delays. The gate is replaced by an equivalent circuit model consisting of a linear voltage source and a linear resistor where their values are determined using empirical factors thus reducing the accuracy. In case the output load is not purely capacitive, an effective capacitance for the RC load is used.

A good and simple approximation of an interconnect line is obtained with the CRC π-model, achieving an accuracy better than 3% in delay calculations in case a P3 model is employed [1]. The π-model becomes more accurate as the capacitance and resistance of the distributed RC line increase. A first attempt to model the interconnect line by a π-circuit was made in [1], however the driving transistor was replaced by a simple resistor. More accurate analytical expressions for the propagation delay and the output waveform can be found if the corresponding system equations of an inverter driving a π circuit are solved. Recently, in [9], an analytical method with emphasis on the short-circuit power dissipation has been presented for an inverter driving an CRC π load. However, the proposed analysis is far too complex to be integrated into a CAD timing analysis system in spite of the simplified assumptions that are made for the short-circuit current.

In this brief, the equivalent π-model is used to capture with higher accuracy the performance of CMOS gates driving RC interconnect loads. The proposed analysis determines the output waveform evolution accurately while keeping the complexity low. In addition, the output waveforms at both ends of an interconnect line are efficiently approximated by piecewise linear waveforms enabling the calculation of the voltage waveform at each point of the interconnect line.

II. Transient Response Analysis

A circuit composed of an inverter driving the equivalent CRC π-model of an interconnect line is considered, where the gate-to-drain coupling capacitance C_m is taken into account (Fig. 1). The α-power law model [4] is used for the transistor current representation and is shown in (1),

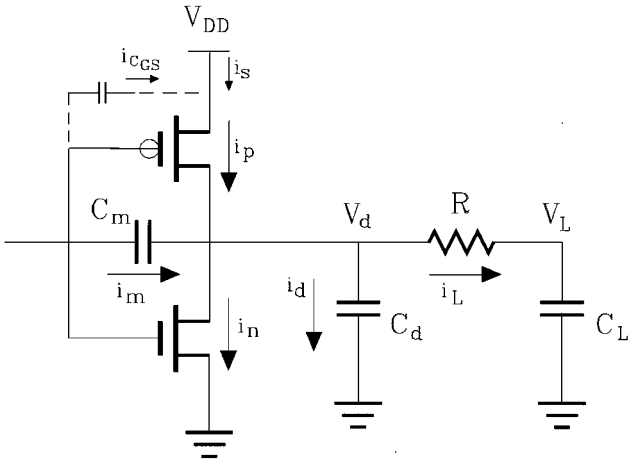

Fig. 1. Inverter driving the π-model of an RC load.

$$I_D = \begin{cases} 0, & V_{\rm GS} \le V_{\rm TO}\text{: cutoff region} \\ k_l(V_{\rm GS}-V_{\rm TO})^{a/2}V_{\rm DS}, & V_{\rm DS} < V_{\rm D-SAT}\text{: linear region} \\ k_s(V_{\rm GS}-V_{\rm TO})^{a}, & V_{\rm DS} \ge V_{\rm D-SAT}\text{: saturation region} \end{cases} \tag{1}$$

where

$V_{\rm D-SAT}$	drain saturation voltage [4];
k_l, k_s	transconductance parameters;
a	velocity saturation index;
$V_{\rm TO}$	zero bias threshold voltage.

A rising ramp input with transition time τ is applied to the transistor gates. The case for a falling ramp is symmetrical. In order to solve the differential equation that describes the operation of the circuit in Fig. 1

$$i_n + i_d + i_L - i_m - i_p = 0 \tag{2}$$

the parasitic current through the pMOS transistor is initially considered negligible. This is a reasonable assumption since long interconnects present a high capacitance thus reducing the maximum value of the short-circuit current [10]. However, at the end of the analysis its influence on the output response will be determined.

Two main cases for input ramps are considered: for fast (slow) inputs, the nMOS device is in saturation (in the linear region) when the input voltage reaches its final value. In order to obtain the output voltage expression analytically, four regions of operation are considered.

A. Fast Input Ramps

Region 1 $(0 < t < t_1)$*:* The nMOS transistor is cut off and differential equation (2) becomes

$$C_2\frac{d^2V_L}{dt^2} + \frac{dV_L}{dt} - C_4 = 0 \tag{3}$$

with initial conditions $V_L(0) = V_{\rm DD}, (dV_L/dt)(0) = 0$ and $C_1 = C_L + C_d + C_m, C_2 = (RC_L(C_d + C_m))/(C_1), C_3 = C_m/C_1$ and $C_4 = C_3V_{\rm DD}/\tau$. The output waveform expression is given by

$$V_L(t) = V_{\rm DD} + C_4t - C_2C_4(1 - e^{-t/C_2}). \tag{4}$$

This expression describes the small overshoot of the output waveform due to the coupling capacitance C_m. This region extends until time $t_1 = V_{\rm TO}\tau/V_{\rm DD}$ where $V_{\rm in} = V_{\rm TO}$.

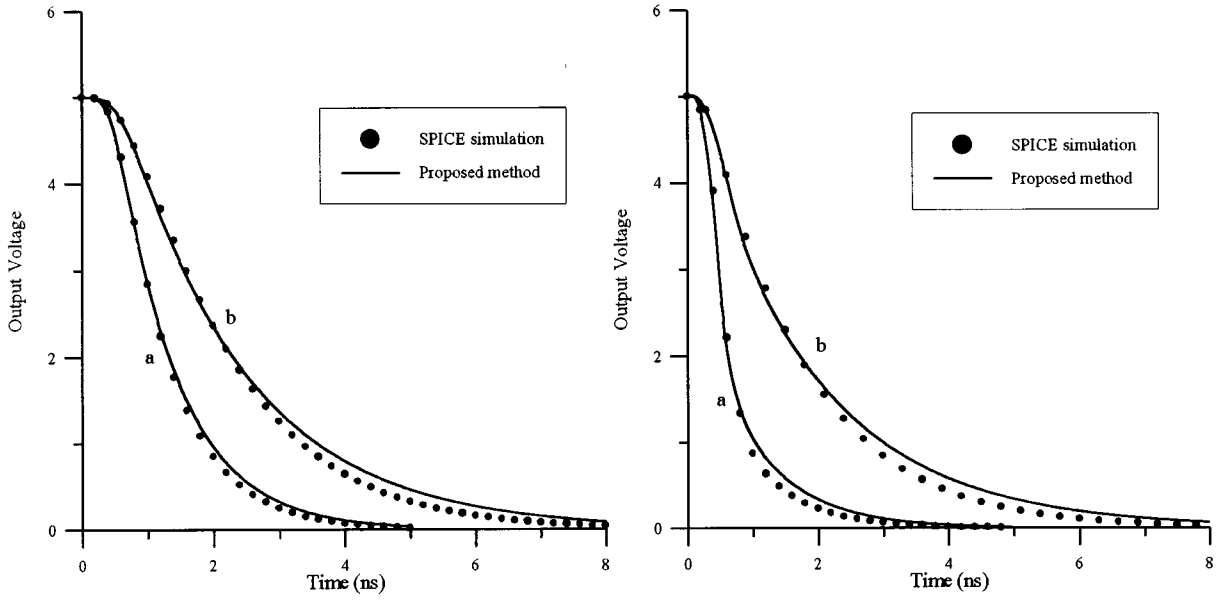

Fig. 2. Output waveform comparison at the end (V_L) and the beginning of the line (V_d) between simulated and calculated values for (a) slow ($\tau = 0.5$ ns, $R = 400\ \Omega, C_d = C_L = 1.5$ pF) and (b) fast ($\tau = 0.5$ ns, $R = 100\ \Omega, C_d = C_L = 5$ pF) cases.

Region 2 ($t_1 < t < \tau$)*:* The nMOS device operates in saturation and the input signal is in transition. Equation (2) becomes

$$C_2\frac{d^2V_L}{dt^2} + \frac{dV_L}{dt} + \frac{k_s}{C_1}\left(\frac{V_{\rm DD}}{\tau}t - V_{\rm TO}\right)^a - C_4 = 0 \qquad (5)$$

which cannot be solved analytically. To obtain an analytical expression for the output, the current term is approximated by a second-order Taylor series at $t = \tau/2$, (where $V_{\rm in} = V_{\rm DD}/2$) with excellent accuracy (error $< 1.5\%$) as $(i_n/C_1) = A_0 + A_1 t + A_2 t^2$. The differential equation is solved, resulting in

$$V_L(t) = C[1] + C_5 t + C_6 t^2 + C_7 t^3 + C[2]e^{-t/C_2} \qquad (6)$$

where $C_5 = C_4 - A_0 + 2C_2((A_1/2) - C_2A_2), C_6 = C_2A_2 - (A_1/2)$, $C_7 = -(A_2/3)$, and $C[1], C[2]$ are the integration constants.

Region 3 ($\tau < t < t_2$)*:* The input has reached its final value and the nMOS transistor is still in saturation. The solution of the circuit differential equation becomes

$$V_L(t) = C[3] - K_1 t + C[4]e^{-t/C_2} \qquad (7)$$

where $K_1 = (k_s/C_1)(V_{\rm DD} - V_{\rm TO})^a$ and $C[3], C[4]$ are the integration constants. This region extends until time t_2 when the nMOS transistor exits saturation. Time point t_2 is calculated by setting the drain-to-source voltage equal to the drain saturation voltage ($V_{\rm D-SATN}$) of the nMOS device:

$$V_d(t_2) = V_L(t_2) + RC_L\frac{dV_L}{dt}(t_2) = V_{\rm D-SATN}(t_2) \qquad (8)$$

where $V_{\rm D-SATN} = (k_s/k_l)(V_{\rm GS} - V_{\rm TN})^{a/2}$[4].

Region 4 ($t > t_2$)*:* The nMOS transistor operates in linear mode and the solution of (2) becomes

$$V_L(t) = C[5]e^{-\frac{1+\sqrt{1-4C_8K_4}}{2C_8}t} + C[6]e^{-\frac{1-\sqrt{1-4C_8K_4}}{2C_8}t} \qquad (9)$$

where $K_2 = (k_l/C_1)(V_{\rm DD} - V_{\rm TO})^{(\alpha/2)}, K_3 = 1 + K_2C_LR, C_8 = C_2/K_3, K_4 = K_2/K_3$.

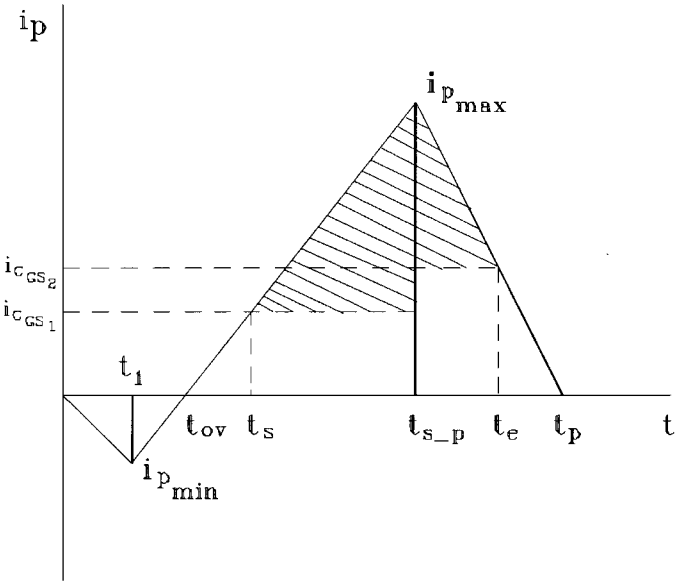

Fig. 3. Representation of the pMOS transistor short-circuit current.

B. Slow Input Ramps

The operating conditions of the structure in regions 1 and 2 are the same as for fast inputs; however, region 2 extends from time t_1 to time t_2, where $t_2 < \tau$.

Region 3 ($t_2 < t < \tau$)*:* The nMOS transistor operates in linear mode while the input is still a ramp. The differential equation describing the output evolution in this region is given by

$$C_2\frac{d^2V_L}{dt^2} + \frac{dV_L}{dt} + \frac{k_l}{C_1}(V_{\rm in} - V_{\rm TO})^{\frac{a}{2}}\left(V_L + RC_L\frac{dV_L}{dt}\right) - C_4 = 0 \qquad (10)$$

which cannot be solved analytically. For this reason, $V_{\rm in}$ is replaced by its average value $\tilde{V}_{\rm in} = (V_{\rm in}(t_2) + V_{\rm DD})/2$. This is a valid approximation since for most of the practical cases the duration of this region

TABLE I
PROPAGATION DELAYS t_d WITH AND WITHOUT THE CALCULATION OF $t_{\rm ad}$. ALL TIMES ARE GIVEN IN ns

			Without t_{ad}			With t_{ad}	
R (Ω)	C (pF)	Actual t_d	Calc. t_d	Error	t_{ad}	$t_d + t_{ad}$	Error
100	3	1.03	1.01	1.94 %	0.024	1.034	0.39 %
	5	1.66	1.64	1.20 %	0.017	1.657	0.18 %
	7.5	2.46	2.43	1.22 %	0.011	2.441	0.77 %
	10	3.25	3.09	4.92 %	0.009	3.099	4.65 %
	15	4.84	4.80	0.83 %	0.007	4.807	0.68 %
400	3	1.65	1.70	3.03 %	0.036	1.736	5.21 %
	5	2.70	2.60	3.70 %	0.018	2.618	3.04 %
	7.5	4.02	3.98	0.99 %	0.012	3.992	0.70 %
	10	5.33	5.10	4.32 %	0.009	5.109	4.15 %
	15	7.96	7.89	0.88 %	0.006	7.896	0.80 %

is very small and thus $V_{\rm in}$ takes values very close to that average value. According to this, the solution of (2) is

$$V_L(t) = \frac{C_4}{K_5} + C[7]e^{-\frac{1+\sqrt{1-4C_9K_6}}{2C_9}t} + C[8]e^{-\frac{1-\sqrt{1-4C_9K_6}}{2C_9}t} \quad (11)$$

where $K_5 = (k_l/C_1)(\tilde{V}_{\rm in} - V_{\rm TO})^{a/2}$, $K_6 = K_5/(1 + K_5RC_L)$, and $C_9 = C_2/(1 + K_5RC_L)$.

Region 4 is solved exactly as for fast inputs.

A comparison of the calculated output response, V_L, with that derived by SPICE simulations is given in Fig. 2(a) for an HP 0.5-μm technology, $W_n = 30\ \mu$m, and $W_p = 50\ \mu$m. The voltage waveform at the output of the driving inverter V_d can be obtained applying Kirchhoff's voltage law in the loop of the π-subcircuit. The accuracy is again sufficient as shown in Fig. 2(b). The small deviation that is observed at the tail of the waveform, which corresponds to the fourth region, is due to the fact that the a-power law model is not as accurate in the linear region as it is in saturation [4]. The propagation delay for a CMOS gate can be calculated as the time from the half-$V_{\rm DD}$ point of the input to the half-$V_{\rm DD}$ point of the output (V_L). Using this definition, the average error in the calculation of propagation delay for several realistic gate and load configurations was found to be around 2%.

III. THE EFFECT OF SHORT-CIRCUIT CURRENT ON PROPAGATION DELAY

In the above analysis, the current through the pMOS transistor was considered negligible. Generally, this is a valid assumption because the capacitive load in long interconnect lines is large enough so that the output voltage does not change significantly until the time the pMOS transistor turns off. This means that the drain-to-source voltage of the pMOS transistor remains small and its current also takes small values. However, the value of the short-circuit current also depends on the width of the driving transistors and the input slope and it may become significant for the case of large drivers and for large input transition times [10]. Therefore, a method for taking into account its influence on the estimation of the propagation delay is presented.

The short-circuit current through the pMOS transistor exists in the interval $[0, t_p]$ where t_p is the time when the pMOS transistor turns off (when $V_{\rm in} = V_{\rm DD} - |V_{\rm TP}|$). A simplified representation of the pMOS current during this period is shown in Fig. 3 [5], [11]. During the output voltage overshoot, which ends at time $t_{\rm ov}$, the pMOS current is negative which means that the current is flowing toward $V_{\rm DD}$. The minimum value of the pMOS current occurs at time t_1 when the nMOS transistor starts conducting. The maximum value occurs when the pMOS transistor enters saturation at time point $t_{\rm s\_p}$. The existence of the pMOS current after time point $t_{\rm ov}$ results in a decrease of the output load discharging current and thus in an increase of the propagation delay. It acts like an amount of charge initially stored at the output node and which has to be removed through the nMOS transistor. On the contrary, the pMOS current before $t_{\rm ov}$ acts as an amount of charge that is being removed from the output load thus it speeds up the output evolution. Consequently, the total equivalent charge Q_e can be calculated by integrating the current of the pMOS device from time 0 to time t_p. If the maximum and minimum value for the pMOS current is calculated and the pMOS current is approximated by linear functions of time [5], then this equivalent charge could be simply obtained as the sum of the area of the two triangles which are set up below and above the time axis.

Since time point t_1 is known and $V_d[t_1]$ was derived in the previous section, the minimum pMOS current can be obtained as $i_{p_{\rm min}} = k_{l_p}(V_{{\rm GS}_p}[t_1] - |V_{\rm TP}|)^{a_p/2}|V_d[t_1] - V_{\rm DD}|$. The time when the pMOS transistor enters saturation is calculated by equating the actual drain-to-source voltage $(V_{{\rm DS}_p})$ to the drain saturation voltage for the pMOS device $(V_{\rm D-SATP})$. Consequently, the maximum pMOS current is calculated as $i_{p_{\rm max}} = k_{s_p}(V_{{\rm GS}_p}[t_{\rm s\_p}] - |V_{\rm TP}|)^{a_p}$. Time $t_{\rm ov}$ is calculated by setting the voltage expression for the inverter output, V_d, in region 2 equal to $V_{\rm DD}$. It should be noted that since the output voltage expression that is used for the calculation of $i_{p_{\rm min}}, i_{p_{\rm max}}$ was extracted without taking into account the short-circuit current, the drain-to-source voltage and consequently the current values at each time point are overestimated. However, this error is small without any significant effect on the overall analysis. According to the above, Q_e can be calculated as

$$Q_e = \frac{1}{2}\left[(t_p - t_{\rm ov}) \cdot i_{p_{\rm max}} - t_{\rm ov} \cdot i_{p_{\rm min}}\right]. \quad (12)$$

In this way, the increase in the propagation delay is found as the time needed to remove the equivalent charge Q_e. The average discharging current, $I_{\rm dch}$, is approximated by the nMOS transistor current at time $t_p/2$, $I_{\rm dch} = i_n[t_p/2]$. The time needed to discharge this extra charge, which causes the additional propagation delay, can be calculated as $t_{\rm ad} = Q_e/I_{\rm dch}$. Table I presents the accuracy that is gained by including the above analysis. It is observed that the short-circuit current effect becomes insignificant as the interconnect capacitance increases.

IV. ESTIMATION OF SHORT-CIRCUIT POWER DISSIPATION

The short-circuit power which is dissipated during the output switching is due to the current i_s (Fig. 1), which is drawn from $V_{\rm DD}$ toward the source of the pMOS transistor. Current i_s can be found by applying Kirchhoff's current law at the source of the pMOS transistor

$$i_s = i_p - i_{C_{\rm GS}} \quad (13)$$

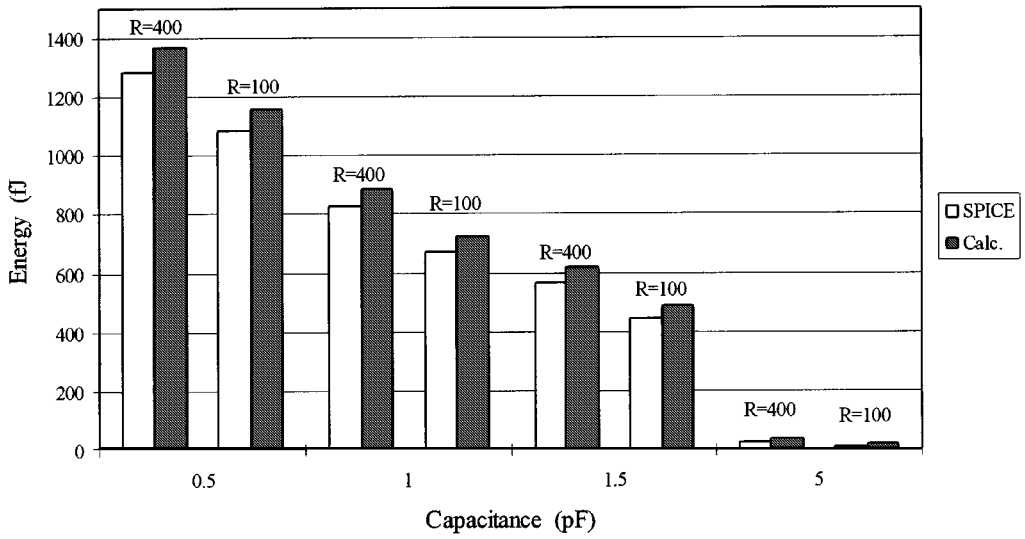

Fig. 4. Comparison between simulated and calculated values for short-circuit energy dissipation, for several capacitances and resistance values (Ω). $\tau = 0.5$ ns.

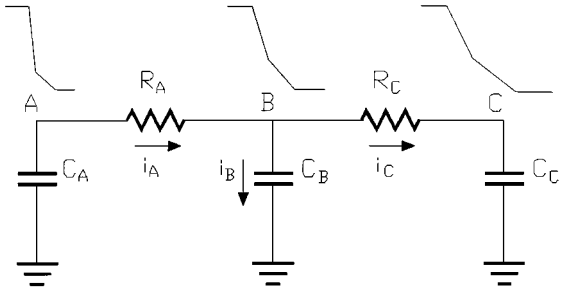

Fig. 5. Voltage waveform evaluation at each point of an interconnect line.

where $i_{C_{\rm GS}} = C_{\rm GS}(dV_{\rm in}/dt) = C_{\rm GS}(V_{\rm DD}/\tau)$ is the current through the gate-to-source coupling capacitance. Since the gate-to-source capacitance has two different values, $C_{\rm GS_1} = (1/2)C_{\rm ox}WL$ in the linear region and $C_{\rm GS_2} = (2/3)C_{\rm ox}WL$ in saturation, where $C_{\rm ox}$ is the gate capacitance per unit area [12], two values will be used for $i_{C_{\rm GS}}$ according to the time point $t_{\rm s\_p}$ (Fig. 3).

Energy begins dissipating at time t_s when i_s starts flowing toward the source of the pMOS transistor so that a current path between $V_{\rm DD}$ and ground exists. Time t_s is calculated by setting $i_s = 0$ in (13) and using the linear approximation for the pMOS current, as shown in Fig. 3. Thus

$$t_s = t_{\rm ov} + \frac{t_{\rm s\_p} - t_{\rm ov}}{i_{p_{\max}}} \cdot i_{C_{\rm GS1}}.$$

The pMOS transistor enters saturation at time point $t_{\rm s\_p}$, where i_p and consequently i_s reach their maximum value. Energy dissipation ceases at time point t_e when $i_s = 0$, after time $t_{\rm s\_p}$. Using the linear approximation for the pMOS current, $t_e = t_p - (t_p - t_{\rm s\_p})/(i_{p_{\max}}) \cdot i_{C_{\rm GS2}}$.

Finally, the dissipated energy due to the short-circuit current during a single transition is

$$\begin{aligned} E_{\rm sc} &= V_{\rm DD}\left(\int_{t_s}^{t_{\rm s\_p}} i_s\,dt + \int_{t_{\rm s\_p}}^{t_e} i_s\,dt\right) \\ &= \frac{1}{2}V_{\rm DD}\left[(t_{\rm s\_p} - t_s)\left(i_{p_{\max}} - i_{C_{\rm GS1}}\right)\right. \\ &\quad \left. + (t_e - t_{\rm s\_p})\left(i_{p_{\max}} - i_{C_{\rm GS2}}\right)\right] \end{aligned} \tag{14}$$

where the integrals are approximated by the shaded area of the corresponding triangles in Fig. 3.

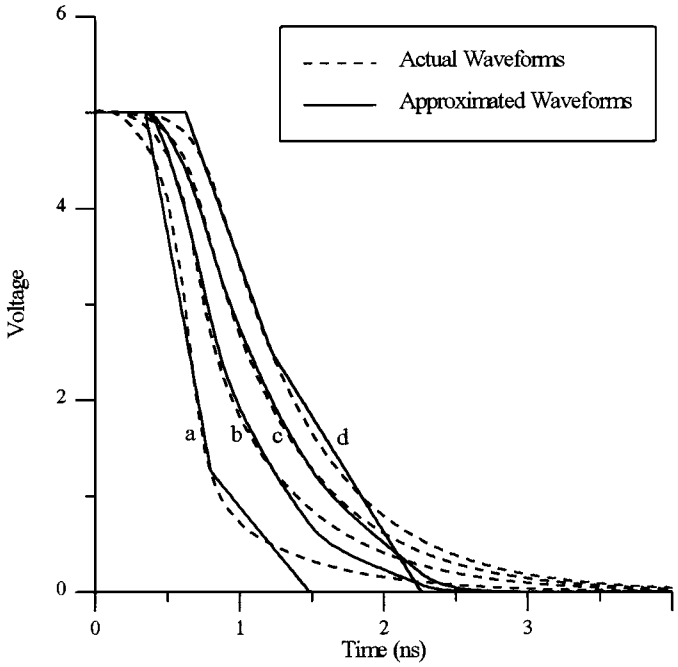

Fig. 6. Output waveform estimation at particular nodes of an interconnect line: (a) at the driving point, (b), (c) at the 25% and 50% point of the line, respectively, and (d) at the end of the line ($R = 800\ \Omega, C = 1.6$ pF, $W_n = 30\ \mu$m, $W_p = 50\ \mu$m, $L = 0.5\ \mu$m, $\tau = 1$ ns).

Consequently, the short-circuit power dissipation for a symmetrical driver is

$$P_{\rm sc} = 2afE_{\rm SC} \tag{15}$$

where α is the switching activity of the output node and f the system clock frequency. In Fig. 4, the actual short-circuit energy dissipated on a CMOS inverter, during a single transition, as measured with SPICE, is compared to the energy which is obtained using the proposed method.

As it can be observed in Fig. 4, the short-circuit energy dissipation decreases as the interconnect capacitance increases. In addition, the short-circuit energy is always larger for higher resistance values. This is due to the shielding effect, which becomes more intense as the resistance increases and leads to a faster discharging at the output of

the inverter. Consequently, the drain-to-source voltage for the short-circuiting device at each time point is larger, resulting in a larger short-circuit current and energy dissipation.

V. Estimating the Voltage Waveform at Each Point of the Line

According to the analysis in Section II, the voltage waveform is known at both ends of the interconnect line. If these two voltage waveforms could be efficiently described by equivalent ramp or piecewise linear waveforms, then the node voltage at each point of the interconnect line could be calculated simply by solving the equation derived by Kirchhoff's current law.

The problem that arises is how to map a real voltage waveform to an equivalent ramp that would incorporate the main characteristics of the initial shape of the waveform. For a waveform appearing at the output of a CMOS gate driving a capacitive load, a very good approximation is a ramp whose slope is equal to 70% of the slope of the actual waveform at the time when the waveform crosses $V_{\rm DD}/2$ [3]. However, the above approach is not valid for waveforms at the output of a gate driving RC loads where nondigital waveform shapes with RC exponential tails are present. In order to find the voltage waveform at each point of an interconnect line, the voltage waveform at the output of the inverter (beginning of the interconnect line) is approximated by a two-piece linear waveform connecting the 90%–25% and 25%–10% points of the waveform. The above points have been selected since the waveform presents a digital behavior with a large slope until low values (for a falling transition) and an RC tail afterward. Since the voltage waveform at the end of the line is generally even more degraded, it is approximated by a two-piece linear waveform connecting the 90%–50% and 50%–20% points. In this way, it is possible to capture again both the main part and the tail of the waveform. Considering the above approximations, the voltage waveform at each point of the line can be obtained as follows: After selecting a point B in the line, two CRC π-circuits can be constructed to model the segments of the line from this point to both ends of the line, marked as A and C. Fig. 5 shows the resulting RC network. Since the waveform at point A is approximated by a piecewise linear waveform as $\tilde{V}_A[t] = k_1 - k_2 t$ and at point C as $\tilde{V}_C[t] = k_3 - k_4 t$ where the coefficients k_1, k_2 and k_3, k_4 are different for each of the two segments of the linear approximation, determining up to five different operating regions, the voltage waveform at point B can be calculated by solving Kirchhoff's current law at node B, resulting in

$$V_B[t] = \frac{m_1 - m_2 t}{(R_A + R_C)^2} + C[x] e^{-\frac{\frac{1}{R_A}+\frac{1}{R_C}}{C_B} t} \tag{16}$$

where $m_1 = (k_3 + C_B k_4 R_C) R_A^2 + (k_1 + k_3) R_A R_C + (k_1 + C_B k_2 R_A) R_C^2 m_2 = (k_2 + k_4) R_A R_C + k_4 R_A^2 + k_2 R_C^2$. The integration constant $C[x]$ will be calculated for each of the regions accordingly. In Fig. 6, the actual waveforms of an interconnect line as obtained with SPICE simulations are compared to the calculated waveforms according to the proposed method. The actual waveforms at both ends of the line and their corresponding two-piece linear approximations are also shown.

VI. Conclusion

An analytical method for the calculation of the output waveform, propagation delay, and short-circuit power dissipation of a CMOS inverter driving an RC interconnect load, modeled as a CRC π-circuit, was introduced. The effect of the short-circuit current on the output waveform evolution is described as an additional charge that has to be discharged to ground. Since the method leads to the output waveforms at both ends of an interconnect line, a further step is introduced in order to calculate the voltage waveform at each point of the line. The calculated results are in very good agreement with SPICE simulation results.

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