TIMING ANALYSIS OF PASS TRANSISTOR AND CPL GATES

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ABSTRACT

Pass Transistor Logic and Complementary Pass-transistor Logic are becoming increasingly important in the design of a specific class of digital integrated circuits due to their speed and power efficiency compared to conventional CMOS logic. A simple and accurate technique for the timing analysis of gates that involve pass transistor logic is introduced. This investigation offers for the first time the possibility to simulate PTL/CPL gates by partitioning the behavior of complex structures into well defined subcircuits whose interaction is separately studied.

I. INTRODUCTION

Pass transistor logic (PTL) and especially complementary pass transistor logic (CPL) have become popular since they offer the possibility to implement high-speed and low power circuits in certain applications. A large number of such circuits has been developed with increased performance in terms of speed and power efficiency [1], [2], as well as synthesis methodologies that target pass transistor implementations [3].

Generally, the use of pass transistor logic leads to reduced transistor count and smaller node capacitances thus decreasing the required area, rise/fall times and power dissipation. However, this circuit style presents the inherent problem of the threshold drop across a transistor which causes static power dissipation in the following stages and imposes the addition of level restoring transistors.

From the implementation point of view, the efficient design of integrated circuits depends strongly on CAD tools that can estimate their performance fast and accurately. Since the transistor count on integrated circuits is increasing there is an intense need for modeling techniques which can offer sufficient accuracy but are orders of magnitude faster than tools based on numerical methods, such as SPICE.

In the recent literature extensive research results for the modeling of static CMOS gates [4], [5], [6] can be found. However, very few modeling techniques for PTL/CPL gates exist such as a delay-macromodeling technique for transmission gates [7]. Existing timing simulators (e.g. ILLIADS[8]) handle pass transistor circuits by mapping pass transistor nodes to simplified primitives by an Elmore time constant approach which is not very accurate. A more efficient technique has been applied in ILLIADS2 [8] which employs waveform relaxation (WR). However, WR is iterative in nature introducing a significant speed penalty while the proposed scheme fails to converge in some cases.

In this paper an accurate and efficient method for the analysis of PTL/CPL gates is introduced. The basic idea behind the proposed approach is that CPL gates can be partitioned into subcircuits which are modeled in a much simpler way.

II. OUTPUT WAVEFORM EVALUATION

A NAND2 gate implemented in CPL [9] (Fig. 1) is considered which forms a basic structure where many characteristics of pass transistor logic can be studied. The gate consists of two nMOS networks corresponding to two signal rails. The two networks are symmetrical and each one consists of two pass transistors controlled by complementary input signals A and $\overline{A}$. One pass transistor is driven by an inverter that belongs to the preceding stage while the other pass transistor is either tied to ground or V_{DD}. Each network is coupled with a pMOS transistor which restores the level of the output signal. 16 possible input combinations exist, depending on whether a signal is V_{DD}, GND, rising or falling ramp (Fig. 2).

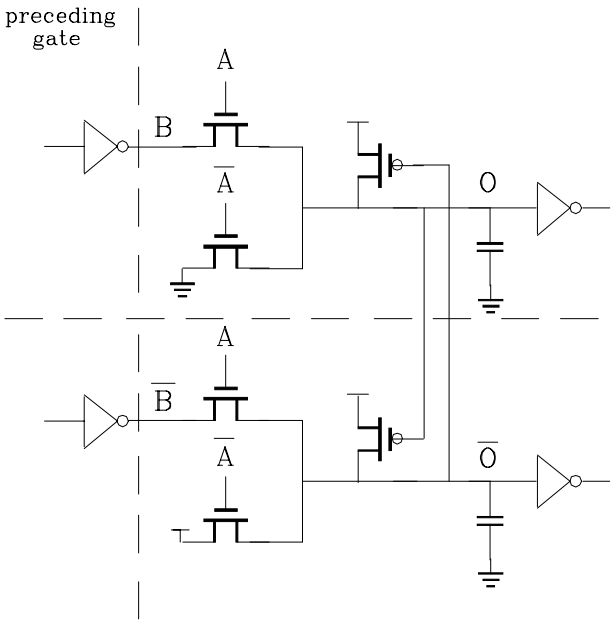


Fig. 1: NAND2 CPL gate

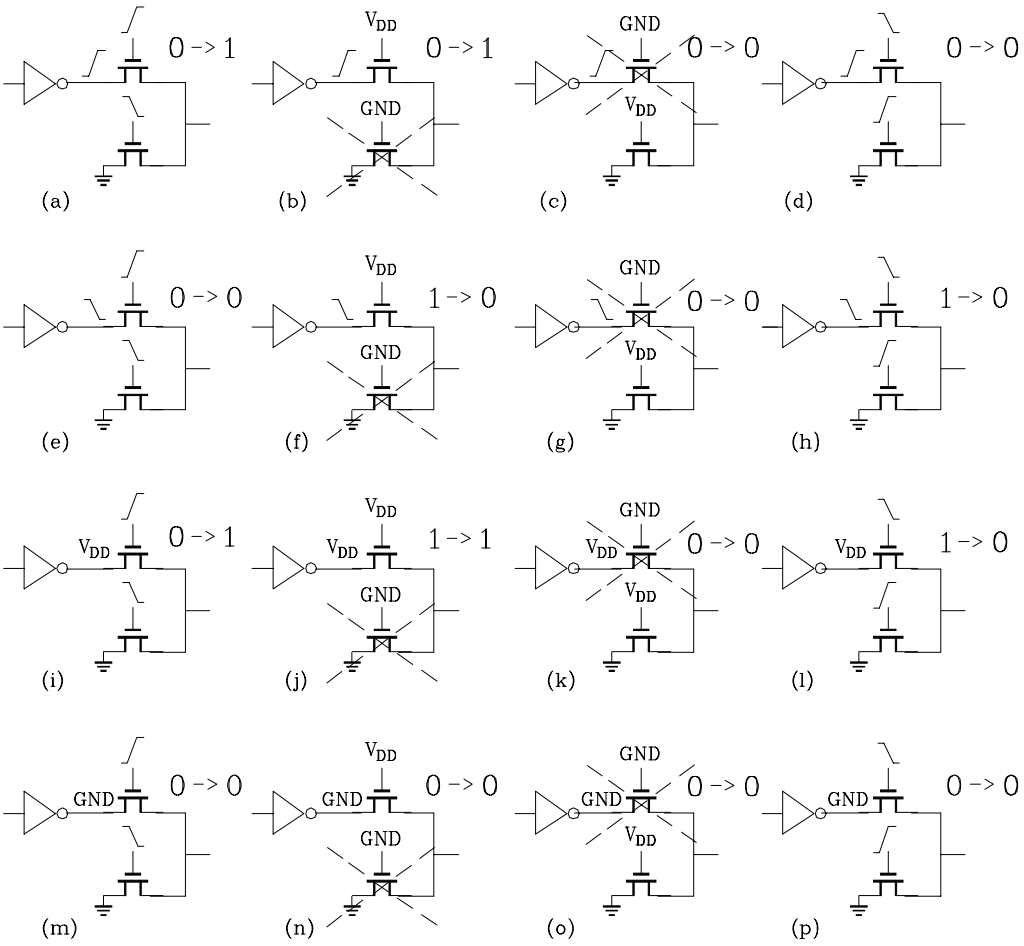
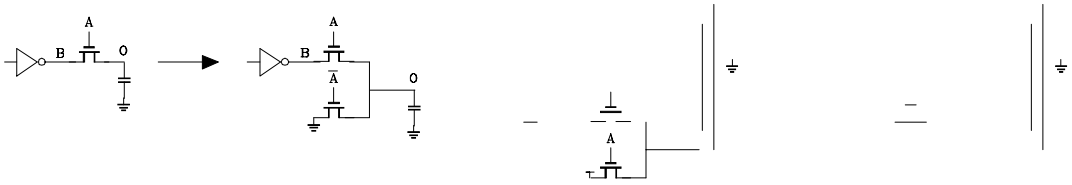


Fig. 2: Input patterns for NAND2 CPL gate


A
B
0
A
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be approximated by a first order Taylor series around $(V_{DD} - V_{TO})/2$ as $V_{TN} = k_1 + k_2 \cdot V_{SB}$ the output waveform at point O is given by :

$$V_{out} = V_g - V_{TN} = g \cdot t - k_1 - k_2 V_{out} \Rightarrow V_{out} = \frac{g \cdot t - k_1}{1 + k_2} \quad (1)$$

b) V_A acts as V_{DD}, case (b). In case V_A acts as V_{DD}, V_B is approximated by a linear function of time with slope s_{inv} and the network output waveform as a linear function of time with slope s_1 which has to be found. Waveform V_B is approximated from the output waveform of the driving inverter by a ramp which crosses the output waveform at $V_{DD}/2$ and has a slope equal to 70 % of the slope of the actual waveform at $V_{DD}/2$ [4]. Moreover, the pass transistor is considered as a resistance since it operates in the linear region and its value is calculated as $R = \frac{1}{k_{l_n}(V_{GS} - V_{TN})^{a/2}}$ at $V_{GS} = (V_{DD} - V_{TN})/2$. The equation at node O becomes :

$$i_n = C_L \frac{dV_{out}}{dt} \Rightarrow \frac{V_B - V_{out}}{R} = C_L \cdot s_1 \Rightarrow \frac{s_{inv} \cdot t - s_1 \cdot t}{R} = C_L \cdot s_1 \quad (2)$$

and calculating the above slope at $t = \tau/2$, where τ is the transition time of V_B ($\tau = V_{DD}/s_{inv}$), leads to : $s_1 = V_{DD}/(2RC_L + \tau)$.

The accuracy of this step is demonstrated in Fig. 4, plots (a), (d) and (g) for cases (i), (b) and (a) respectively. In these plots the simulated and calculated output waveform of a single pass transistor which is driven by an inverter is shown for a 0.5 μm HP technology.

Step 2: *Incorporation of short-circuit pass transistor effect*

The next step is to consider the effect of the nMOS transistor, M_{gnd}, which has one terminal connected to ground (top subcircuit in Fig. 1a). In case the gate signal A is considered as V_{DD} compared to V_B, the gate signal $\overline{A}$ of transistor M_{gnd}, will effectively act as GND and the transistor will be cut-off without having any effect on the output waveform at point O (case (b)). In case the gate signal A cannot be considered as V_{DD} it is reasonable to assume that up to a time point, transistor M_{gnd}

will be conducting, thus draining the capacitance charging current to ground. Consequently, up to this time point, t_s, which was found to be close to the time when the gate signals reach $V_{DD}/2$, the output voltage remains at its initial value. The starting point of the output waveform which was calculated in Step 1 has to be shifted to time point t_s. However, the ending time point of the output waveform remains unchanged resulting in a steeper increase of the output voltage. In plots (b), (e) and (h) of Fig. 4, the simulated and calculated output waveform of a network of a CPL gate (excluding the pMOS restoring transistor) is shown.

Step 3: ***Incorporation of the pMOS transistor restoring effect***

In this step, the effect of the pMOS restoring transistor on the output waveform at point O is considered. This transistor is driven by the output of the symmetrical network $\overline{O}$ which in turn is approximately the symmetrical waveform of point O. Consequently, up to the time point when the pMOS transistor starts conducting strongly (the time when $\overline{O}$ reaches the 50% point) the output at point O is that determined in step 2. From this point on, the pMOS transistor pulls the output voltage to V_{DD} contributing to a faster charging rate of the output capacitance which can be captured accurately by increasing from this point on the slope of the output and is calculated as follows :

a) V_A **acts as** V_{DD}. Let us consider a single pass transistor driving an output load and a pMOS restoring transistor. Since the nMOS pass transistor operates in the linear region it can be considered as a resistance R while the input waveform is approximated by a ramp with slope s_{inv} and the output waveform by a ramp with slope s_3. Since the gate of the pMOS restoring transistor in a CPL gate is driven by the output of the symmetrical network, it is assumed that $|V_{GS}| = |-V_{out}|$. The pMOS transistor operates in the linear region and the differential equation at the output is:

$$i_n + i_p = C_L \frac{dV_{out}}{dt} \Rightarrow \frac{s_{inv}t - s_3 t}{R} + k_{l_p}\left(s_3 t - V_{TP}\right)^{a_p/2}\left(V_{DD} - s_3 t\right) = C_L s_3 \qquad (3)$$

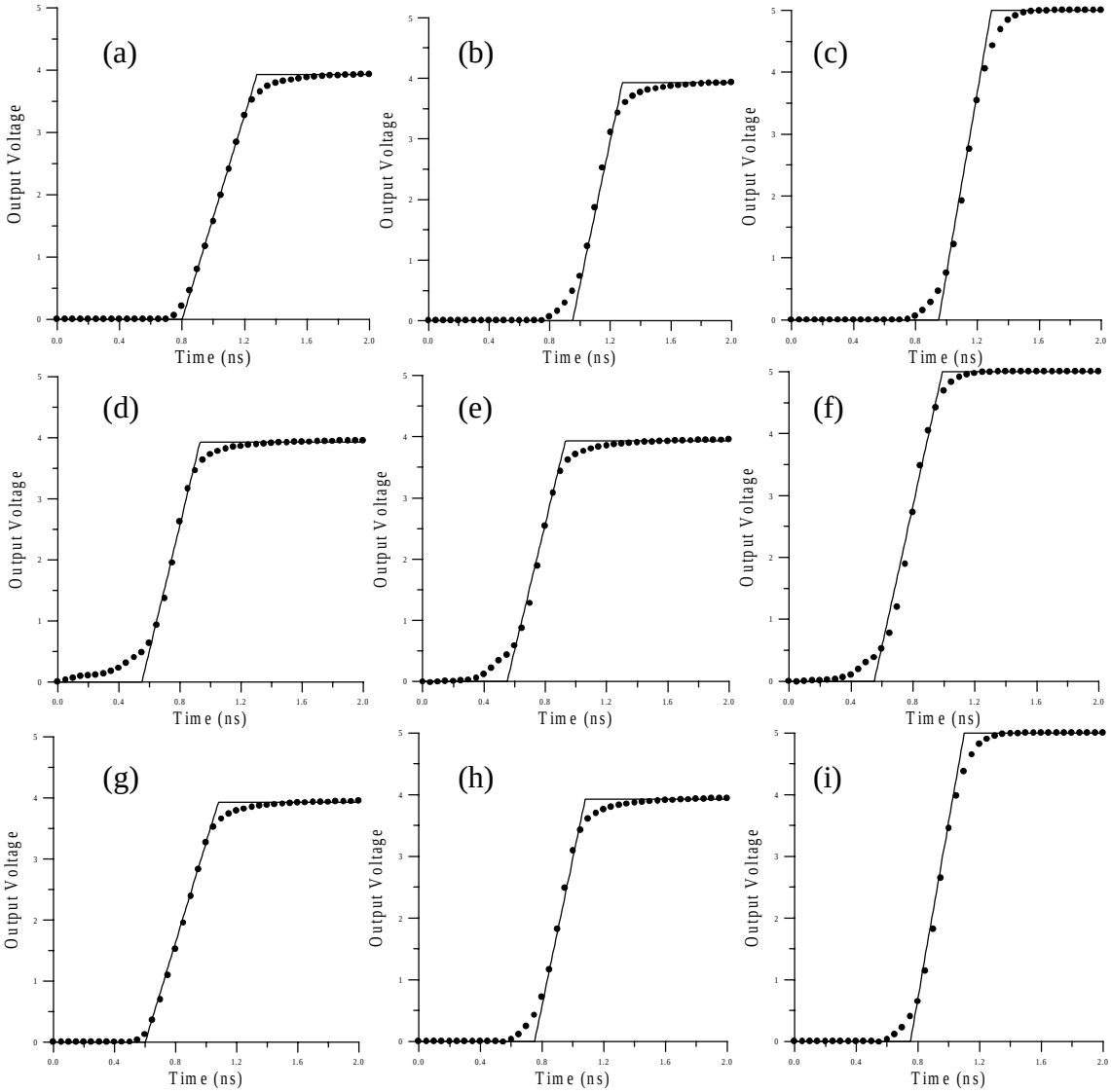

Fig. 4: Output waveform comparison between simulated (dots) and calculated results for the three steps of the NAND2 output estimation. (a)-(c): **case (i)**, (d)-(f): **case (b)**, (g)-(i): **case (a)**

From the above equation the slope of the output waveform can be calculated as a function of time. Calculating the slope at $3\tau/4$ gives sufficiently accurate results. Once the output waveform at step 2 is obtained, the slope of the output waveform after the time when the output reaches $V_{DD}/2$ should be increased to s_3.

b) V_A does not act as V_{DD} . In this case, the gate-to-source voltage V_{GS} of the pass transistor is small since the output voltage "follows" the gate signal. Consequently the current through the pass transistor is extremely small and after the pMOS transistor starts conducting strongly the output voltage is determined only by the current of the pull-up pMOS device. The increased slope is obtained by solving :

$$i_p = C_L \frac{dV_{out}}{dt} \Rightarrow k_{l_p} \left(s_3 t - V_{TP} \right)^{a_p/2} \left(V_{DD} - s_3 t \right) = C_L s_3 \quad (4)$$

s_3 is calculated at $t = 3\tau/4$. In Fig. 4, plots (c), (f) and (i), simulated and calculated results are shown for a complete network including the restoring pMOS transistor.

Step 4: ***Obtaining the gate output waveform***

The gate output waveform is obtained by performing transient analysis on the output inverter using analytical [4], [5] or macromodeling techniques having the network output waveform that has been obtained as input to the inverter.

B. Cases (h), (l)

The transistor which has its source node tied to ground is becoming increasingly conducting since it receives a rising input ramp as a gate signal. The other pass transistor is poorly conducting because its V_{GS} is throughout the output evolution close to zero. Consequently, the pass transistor node which is driven by the inverter of the preceding stage does not have any significant effect on the output waveform. The output waveform is obtained by solving the differential equation describing the discharging of a capacitance through an nMOS transistor.

To capture the effect of the pMOS restoring transistor (step 3), it is considered that the pMOS current acts as an additional charge at the output node which has to be discharged to ground slowing down the output discharging. A rough estimation of this additional charge can be performed as follows. The maximum value of the pMOS current, occurs around the point when both its V_{GS} and V_{DS} are at the half V_{DD} point. Consequently, $I_{pmax} = k_{l_p} \left(\frac{V_{DD}}{2} - V_{TP} \right)^{a_p/2} \frac{V_{DD}}{2}$, where V_{TP} is the threshold voltage of the pMOS transistor. The current is almost symmetrical around this point which is close to the time where the pMOS transistor enters saturation and it is represented by a piece-wise linear function [10]. Assuming for simplicity that the output evolution lasts as much as the gate signal transition, the additional charge can be approximated as $Q_{ad} = I_{pmax} \cdot \left(V_{DD} - V_{TP} \right) \tau / \left(2 V_{DD} \right)$

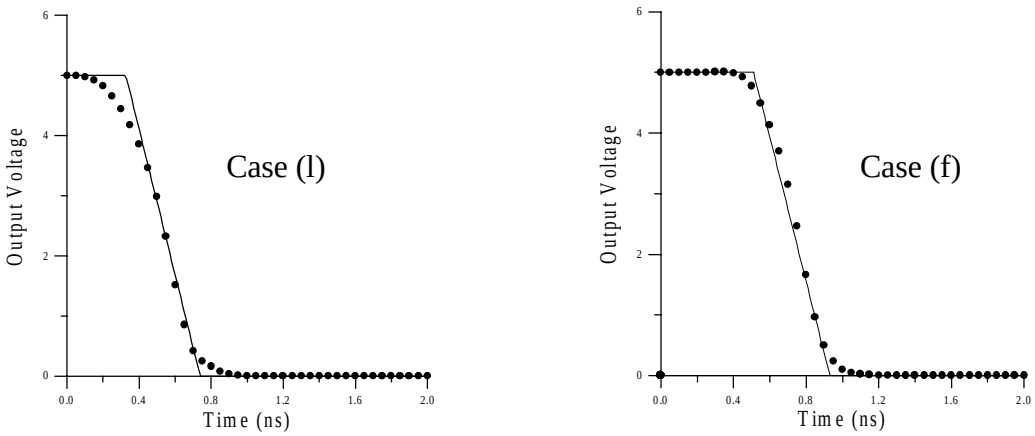

Fig. 5: Output waveform comparison between simulated (dots) and calculated results

where τ is the transition time of the gate signal. Since the initially stored charge at the output capacitance is $Q_{init} = C_L V_{DD}$, the additional charge can be considered as an increase of the output node capacitance by $C_{ad} = Q_{ad}/V_{DD}$. If this capacitance is added to C_L and the output waveform is calculated, it matches that of the actual CPL network with very good accuracy (Fig. 5) (case (h) has the same response).

C. Case (f)

The pass transistor which has its source node connected to ground is cut-off. The output load will be discharged through the other pass transistor and the pMOS restoring transistor has the same effect as in the previously described cases (h), (l) and thus can be captured by an increased output node capacitance which is taken into account when the output of the driving inverter is calculated. Finally, to obtain the output waveform at point O, since the pass transistor starts conducting when the input voltage at the source node drops to V_{DD}-V_T, at this time point the output should start being discharged. The ending time point remains unchanged (Fig. 5).

D. Other cases - Synopsis

For all other cases no transition on the output occurs independently of the applied inputs and thus no analysis is required. The network which includes a pass transistor connected to V_{DD} can be studied exactly in the same way, since all possible input patterns correspond to the already presented cases in Fig. 2.

Other pass-transistor structures such as XOR CPL gates and MUXes can be modeled according to the methodology that has been developed for the NAND2 gate. All possible input patterns correspond either directly to a NAND2 CPL gate or do not lead to a transition at the output node.

III. CONCLUSION

An efficient and accurate methodology for modeling logic styles that employ pass transistor structures has been introduced. It is shown that a NAND2 CPL gate can be analyzed by partitioning a circuit according to the distinct sub-circuits that coexist. The output waveform extraction involves only a few simple mathematical operations enabling the analysis of pass-transistor structures at fast times.

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