EFFICIENT OUTPUT WAVEFORM EVALUATION OF A CMOS INVERTER

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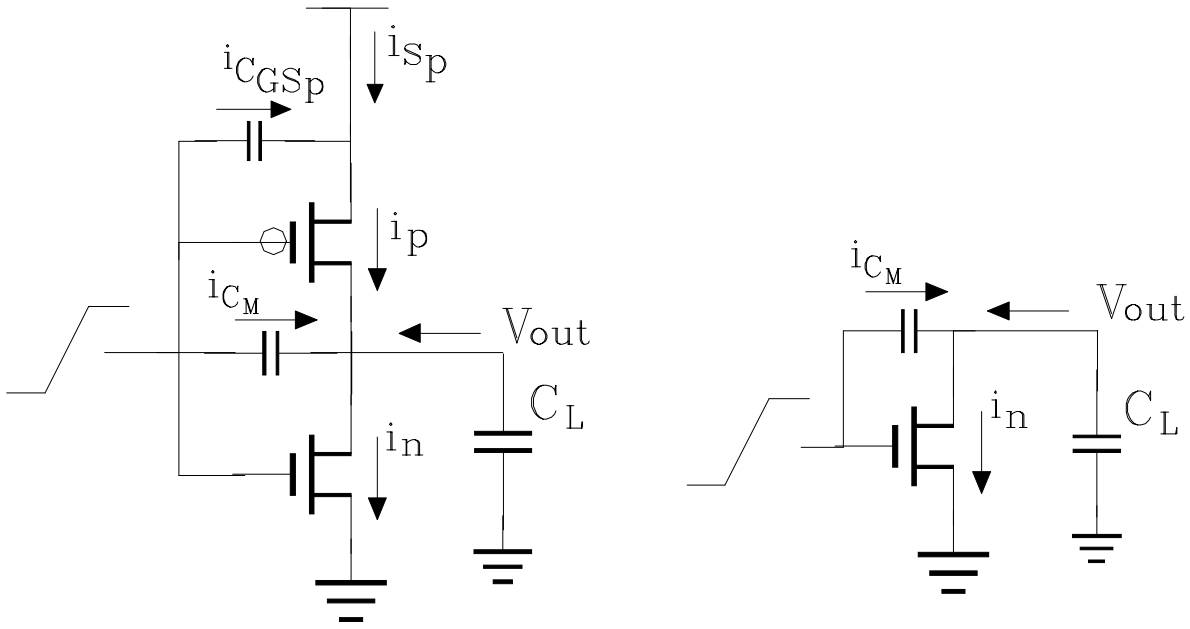
ABSTRACT

A novel approach for obtaining the output waveform, the propagation delay and the short-circuit power dissipation of a CMOS inverter is introduced. The output voltage is calculated by solving the circuit differential equation only for the conducting transistor and the effect of the short-circuit current is considered as an additional charge which causes a shift of the output waveform. A tool has been implemented on this method and the results prove that a significant speed improvement can be gained without significant loss in accuracy.

I. INTRODUCTION

The development of digital integrated circuits with short design cycles requires accurate and fast timing and power simulation. Unfortunately, simulators such as SPICE are excessively slow for large designs. The need for analytical methods which can produce accurate results at short times is obvious and extended research has been conducted for the CMOS inverter [1]-[5] which forms a basic block to which all CMOS structures can be diminished.

Modeling techniques at the inverter level are very accurate but this comes at the cost of increased complexity. The analysis of the inverter is complicated mainly due to the presence of the short-circuit current which acts parasitically on the



(a) (b)

Fig. 1: (a) Actual inverter, (b) conducting transistor

output evolution. The circuit differential equation has to be solved taking into account the current of both the pMOS and the nMOS transistor. This leads to complicated expressions for the output waveform increasing significantly the execution time.

In this paper a method to avoid the intricacy of the short-circuit current by solving the differential equation that describes the circuit considering only the conducting transistor is introduced. The effect of the short-circuit current is taken into account as an additional charge which has to be discharged through the conducting transistor.

II. OUTPUT WAVEFORM EVALUATION

Let us consider the inverter of Fig. 1a whose operation is described for a rising input ramp with transition time τ by the following differential equation:

$$C_L \frac{dV_{out}}{dt} = i_{C_M} + i_p - i_n \qquad (1)$$

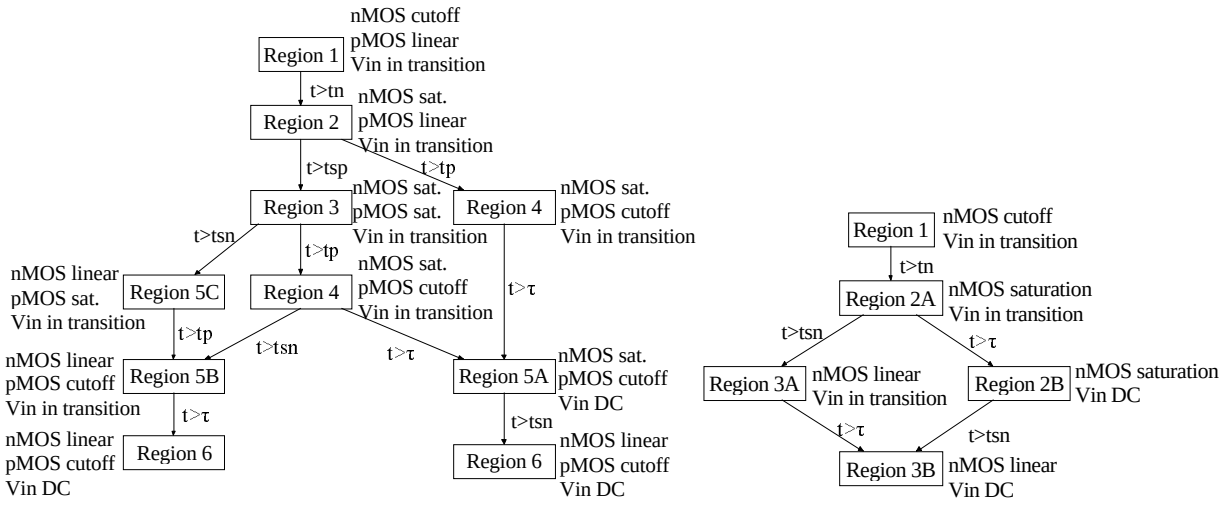


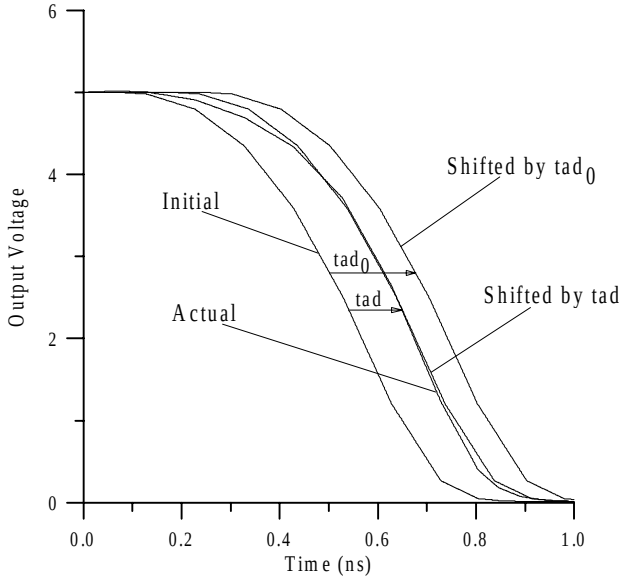
Fig. 2: Decision diagrams for (a) fully analytical and (b) proposed method

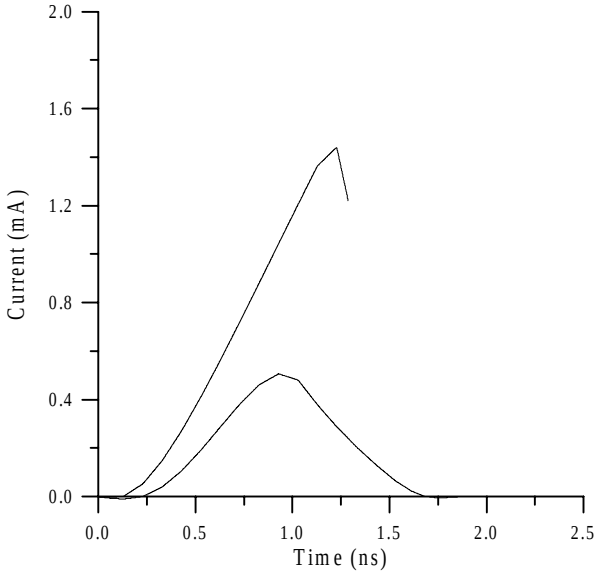
where $i_{C_M} = C_M\left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt}\right)$ is the current through the coupling capacitance C_M between input and output. The case of a falling input ramp is symmetrical. If the short-circuit current i_p is neglected (Fig. 1b), the output waveform can be obtained by solving the above equation according to the region of operation of the conducting nMOS transistor. This waveform will be referred to as initial waveform, $V_{out_{init}}(t)$. For submicron devices the output is obtained with excellent accuracy using the alpha-power law model for the nMOS transistor current [3] :

$$I_D = \begin{cases} 0 & V_{GS} \le V_{TN} \ : cutoff\ region \\ k_l\left(V_{GS} - V_{TN}\right)^{a/2} V_{DS} & V_{DS} < V_{DSAT} \ : linear\ region \\ k_s\left(V_{GS} - V_{TN}\right)^{a} & V_{DS} \ge V_{DSAT} \ : saturation\ region \end{cases} \quad (2)$$

where V_{DSAT} is the drain saturation voltage, k_l , k_s the transconductance parameters, α the carrier velocity saturation index and V_{TN} is the threshold voltage.

Calculating the output waveform considering only the conducting current leads not only to simpler expressions for the output waveform and thus to faster execution time but is also substantially more simple in terms of program complexity. In Fig. 2 the decision diagrams and the operating regions through


Output Voltage
Time (ns)
Initial
Actual
Shifted by tad0
Shifted by tad
tad0
tad
0
2
4
6
0.0
0.2
0.4
0.6
0.8
1.0


Current (mA)
Time (ns)
0.0
0.4
0.8
1.2
1.6
2.0
0.0
0.5
1.0
1.5
2.0
2.5

nMOS current are calculated on V_{out} and result as functions of the additional delay. Therefore, t_{ad}, can be obtained by solving:

$$t_{ad} = \frac{Q_{ad}(t_{ad})}{I_{dch}(t_{ad})} \tag{3}$$

Consequently, the key point in the proposed method is the accurate approximation of the transistor currents as simplified functions of the additional delay, t_{ad}.

The actual pMOS short-circuit current can be approximated by a piece-wise linear function of time [4], [5] (Fig. 3b). The charge that it contributes can easily be calculated as the area of the corresponding triangle which is equal to $Q_{ad} = I_{pmax}(t_e - t_s)/2$. $I_{p_{max}}$ is the maximum value of the pMOS current and occurs when the pMOS transistor enters saturation at $t=t_{sp}$. The time at which the pMOS current is considered to start, is $t_s = t_n$ where $t_n = \frac{V_{TN}}{V_{DD}}\tau$ is the time when the nMOS transistor starts conducting. The reason for which this time point is selected is that the pMOS current presents initially an undershoot. The undershoot occurs due to the coupling capacitance between input and output which in turn causes an overshoot in the output voltage forcing the output node of the inverter to be at a higher potential than V_{DD} [2], [4], [5], [6]. During the overshoot current is flowing towards V_{DD} causing the undershoot of the pMOS current. The minimum pMOS current occurs close to $t=t_n/2$ when a subthreshold current starts flowing through the nMOS transistor. The undershoot was found to cease close to $t=t_n$. The pMOS current ceases at time $t_e = (V_{DD} - V_{TP})\tau/V_{DD}$, where V_{TP} is the threshold voltage of the pMOS transistor. Time point t_{sp_0} when the pMOS transistor enters saturation according to the initial output waveform is found by solving $V_{DSAT_p}(t) = \left|V_{out_{init}}(t) - V_{DD}\right|$ where V_{DSAT_p} is the drain saturation voltage of the pMOS transistor [3]. Using linear approximations for $V_{DSAT_p}(t)(\approx s_1 - s_2 t)$ and $V_{out_{init}}(t)$ $(\approx p_1 - p_2 t)$, t_{sp} can be expressed as a function of t_{sp_0} and t_{ad} :

$t_{sp} = t_{sp_0} + g\, t_{ad}$ ($g = \dfrac{p_2}{p_2 + s_2}$). According to the above :

$$I_{p\,max} = k_{s_p}\left(V_{DD} - V_{in}\left[t_{sp_0} + g\, t_{ad}\right] - \left|V_{TP}\right|\right)^{a_p} \tag{4}$$

where k_{s_p} is the transconductance of the pMOS transistor in saturation.

Similarly, the time when the nMOS transistor exits saturation in the actual inverter is equal to $t_{sn} = t_{sn_0} + h\, t_{ad}$ ($h = \dfrac{r_2}{r_2 + q_2}$) where t_{sn_0} is the time when the nMOS transistor exits saturation for the initial waveform and is found by solving $V_{out_{init}}(t) = V_{DSAT_n}(t)$ ($V_{DSAT_n}(t) \approx q_1 + q_2\, t$ is the drain saturation voltage of the nMOS transistor and $V_{out_{init}}(t) \approx r_1 - r_2 t$).

The effect of the pMOS current is to prolong the saturation region of the nMOS transistor resulting in an increase of its current (Fig. 3b). Therefore, the discharging current of the additional charge which determines the time shift of the initial output waveform is approximated by the average of the maximum nMOS current that corresponds to V_{out} and that corresponding to the initial waveform :

$$I_{dch} = \left(k_{s_n}\left(V_{in}\left[t_{sn_0} + h\, t_{ad}\right] - V_{TN}\right)^{a_n} + k_{s_n}\left(V_{in}\left[t_{sn_0}\right] - V_{TN}\right)^{a_n} \right) / 2 \tag{5}$$

where k_{s_n} is the transconductance of the nMOS transistor in saturation.

Since currents are almost linear functions of time [4] equation (3) can be solved for t_{ad} with sufficient accuracy using first order Taylor series approximations for the pMOS and nMOS currents around the point $t_{ad} = t_{ad_0} / 2$.

III. SHORT-CIRCUIT POWER ESTIMATION

Since the form and the magnitude of the pMOS current in the above analysis is obtained, the proposed method can also be used in order to calculate the short-circuit energy which is dissipated when the output of an inverter switches state. The dissipated short-circuit energy during output discharging is calculated as :

$$E_{SC}^{d} = V_{DD} \cdot \int_{t_s}^{t_e} i_{s_p}(t)\, dt \tag{6}$$

The short-circuit energy dissipation during output charging, E_{SC}^{c}, can be obtained in a symmetrical way.

However, the current that is causing the short-circuit power dissipation, i_{s_p}, is not the pMOS transistor current but the current that is flowing from V_{DD} towards the source of the pMOS transistor [7] (Fig. 1a). In order to calculate this current, the Kirchhoff's current law has to be applied at the source node of the pMOS transistor, which gives:

$$i_{s_p} = i_p - i_{C_{GSp}} \tag{7}$$

where $i_{C_{GSp}}$ is the current through the gate-to-source capacitance C_{GS_p} and is given by $i_{C_{GSp}} = C_{GS_p} \dfrac{dV_{in}}{dt}$.

Since the integral $\int_{t_s}^{t_e} i_p(t)\, dt$ is the charge Q_{ad} that has already been calculated, the short-circuit energy dissipation can be easily approximated as:

$$E_{SC}^{d} = V_{DD} \cdot \left(Q_{ad} - i_{C_{GSp}} \cdot (t_e - t_s)\right) \tag{8}$$

IV. RESULTS

A tool has been implemented that calculates the output waveform of a CMOS inverter based on a fully analytical solution [2] while another one implements the proposed technique. The proposed technique was found to be about 10 times faster than the fully analytical solution. Accuracy comparisons with SPICE for a 0.5 μm HP technology and the corresponding execution times for the analysis of an inverter are shown in Table I for several input transition times and load capacitances (W_n=4μm, W_p=6μm). As it can be observed, a significant speedup can be gained with a minor penalty in accuracy.

Table I: Accuracy and speed comparison between calculation and SPICE

τ (ns)	C_L (fF)	*Prop.Delay SPICE* (ns)	*Prop.Delay Calc.* (ns)	*Error (%)*	*Exec.Time SPICE* (secs)	*Exec.Time Calc.* (secs)	*Speedup*
0.5	50	0.076	0.071	6.58	0.23	0.00164	140
0.5	100	0.129	0.127	1.55	0.16	0.00156	103
1	50	0.061	0.059	3.28	0.19	0.00181	105
1	100	0.138	0.135	2.17	0.16	0.00173	92
2	100	0.113	0.109	3.54	0.15	0.00208	72
2	200	0.263	0.268	1.90	0.27	0.00191	141

A widely accepted dynamic timing simulator is ILLIADS2 [8], [9] which employs regionwise quadratic modeling (RWQ) for capturing of submicron MOS current models. Execution times for the simulation of an inverter by SPICE, ILLIADS2, the fully analytical method and the proposed method are given in Fig. 4 for several input transition times/output loads. It is obvious that the proposed method is much faster than SPICE and significantly more efficient than ILLIADS2 and the fully analytical method.

It is important to mention that for timing purposes it is sufficient to know the time when the output waveform crosses $V_{DD}/2$ and its slope at this point, so that this waveform can be approximated by a ramp in order to feed it to the next stage [1]. The proposed method, although not very accurate at the beginning and the tail of the output waveform, is very accurate around the 50% point (error in slope less than 3%) and consequently is appropriate for use in timing simulators. When the complete output voltage waveform is not required, only the propagation delay and the slope at $V_{DD}/2$ are calculated [1] resulting in a speedup of more than $2 \cdot 10^3$.

The calculated energy for a single output transition according to the method of the previous section lies very close to the energy which is measured from SPICE

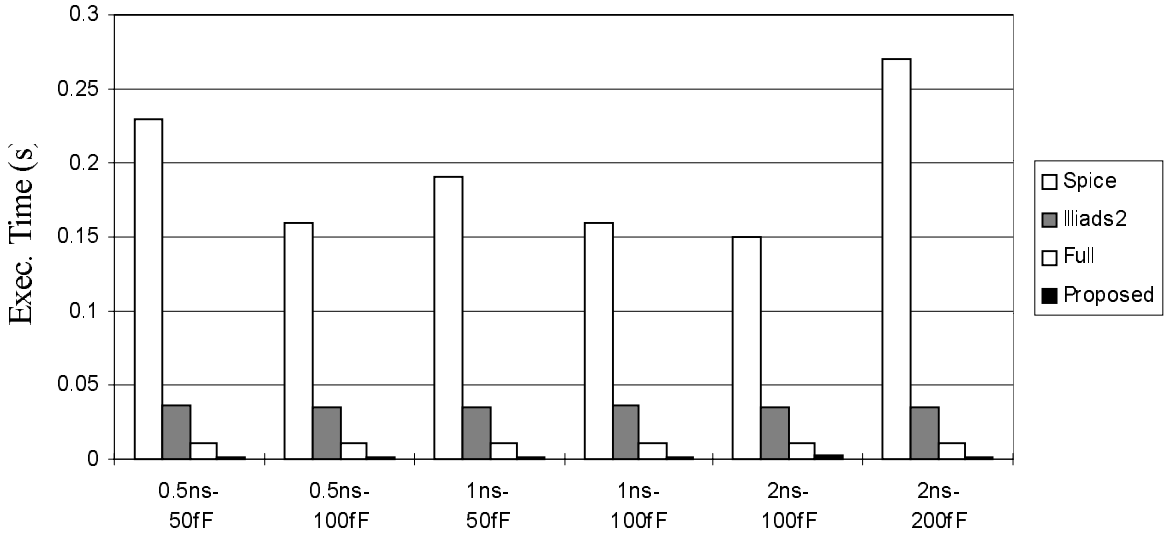


Fig. 4: Execution times of several simulation tools (.TRAN 0.01ns 5ns)

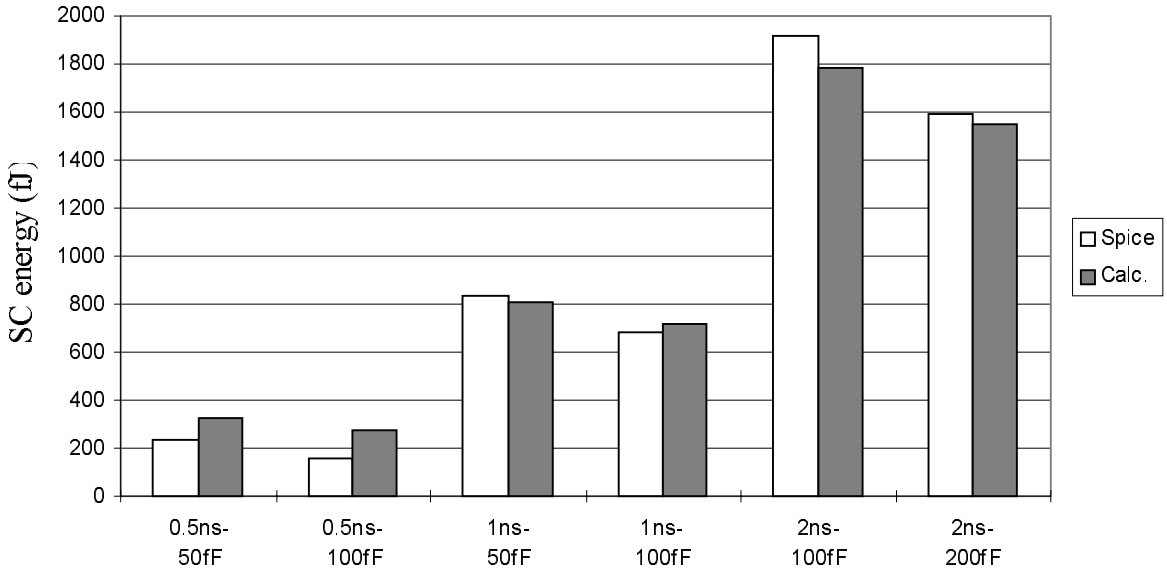


Fig. 5: Simulated and calculated short-circuit energy dissipation

simulations. In Fig. 5 a comparison of the calculated and simulated short-circuit energy values during output discharging is shown for an inverter and for several input transition times/output loads. Using SPICE, the short-circuit power dissipation can be obtained by integrating the current at the source terminal of the pMOS transistor or by using a power meter [10].

V. CONCLUSION

A method for improving the efficiency of the simulation of the CMOS inverter by avoiding to take into account the short-circuit current in the solution of the circuit differential equation has been introduced. The effect of the short-circuit current is considered as an additional charge which causes a shift of the output waveform. The proposed method is faster than any other existing analytical technique while accuracy is maintained.

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