SINGLE TRANSISTOR PRIMITIVE FOR MODELING CMOS GATES

A. Chatzigeorgiou, S. Nikolaidis [1] *and I. Tsoukalas*

Computer Science Department, [1]Department of Physics

Aristotle University of Thessaloniki, 54006 Thessaloniki, Greece

email: achat@skiathos.physics.auth.gr

ABSTRACT

An accurate and efficient method for modeling CMOS gates by a single equivalent transistor is introduced in this paper. The proposed macromodel, which takes into account the effect of the short-circuit current, is the simplest primitive that can be used in order to obtain the output waveform and the propagation delay of CMOS gates. Consequently it can offer significant speed improvement to existing dynamic timing simulators while maintaining a sufficient level of accuracy.

1. INTRODUCTION

The development of digital integrated circuits with short design cycles imposes the use of fast and accurate verification tools. It has been extensively pointed out that with shrinking device dimensions and increasing number of transistors on integrated circuits in the submicron era, the difficulty in performing efficient simulation of these circuits is increasing. In contrast to numerical approaches such as SPICE, for calculating propagation delay and power dissipation, analytical methods can offer a significant speed improvement, assuming that accurate models which can describe the behavior of transistor structures exist.

The simplest representation of static logic gates that has been presented in the literature is the equivalent inverter of a gate [1], [2], [3], [4] which if calculated properly can estimate the performance of complex gates with very good accuracy, thus enabling the timing analysis of digital integrated circuits at a lower level of complexity. In this way macromodels or accurate analytical techniques have to be developed only for the corresponding inverters [5], [6], [7]. However, the analysis at the inverter level remains complicated due to the nature of the differential equation that governs its operation resulting in a relatively large runtime penalty [5].

In this work the previous approach is extended in order to obtain a single transistor which models accurately the behavior of an inverter. The short-circuit current reduces the 'effective' charging/discharging output current thus increasing the propagation delay as it slows down the output evolution. The effect of the short-circuit current from a different point of view can be considered as a differentiation (reduction) of the actual driving transistor width in order to charge/discharge the output load at a slower pace. The accurate calculation of the driving transistor width according to the region of operation of the short-circuiting device will be presented in the rest of the paper and its efficiency and accuracy will be shown.

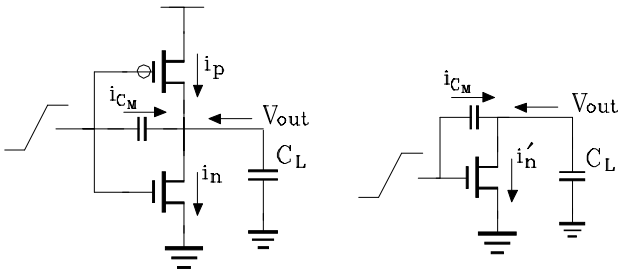
The use of a much simpler primitive for modeling CMOS gates reduces the computational complexity in two ways. First the form of the differential equation becomes simpler and consequently the solution. Moreover, the differential equation of an inverter cannot be solved for some regions (being a Ricatti-like equation) imposing the use of many series approximations which increase the execution time and reduce the accuracy.

2. PROPOSED MACROMODEL

Let us consider the inverter of Fig. 1a to which a rising input ramp with transition time τ is applied and a single transistor driving the same load (Fig. 1b) whose width is to be calculated so that its output response match that of the inverter when the same input is applied. The gate to drain coupling capacitance C_M is also shown in Fig. 1. For the equivalent transistor the coupling capacitance should take into account the gate-to-drain capacitances of both transistors. The alpha power law model [8], which takes into account the carrier velocity saturation effect of short-channel devices, will be used for the transistor currents since it is the most accurate model for submicron devices (the equations correspond to the nMOS transistor) :

$$I_D = \begin{cases} 0 & V_{GS} \le V_{TN} \ : cutoff \\ k_l \left(V_{GS} - V_{TN}\right)^{a/2} V_{DS}, & V_{DS} < V_{D-SAT} \ : linear \\ k_s \left(V_{GS} - V_{TN}\right)^{a} & V_{DS} \ge V_{D-SAT} \ : sat. \end{cases} \quad (1)$$

where $V_{D\text{-}SAT}$ is the drain saturation voltage [8], k_l , k_s are the transconductance parameters which depend on



(a) (b)

Fig. 1: (a) CMOS Inverter and (b) Single Transistor Primitive

the width to length ratio of a transistor, α is the carrier velocity saturation index and V_{TN} is the threshold voltage.

The differential equations that govern the behavior of the two circuits are :

$$i_p - i_n = C_L \frac{dV_{out}}{dt} - i_{C_M} \quad \text{(inverter)} \qquad (2)$$

$$i'_n = -C_L \frac{dV_{out}}{dt} + i_{C_M} \quad \text{(equiv. transistor)} \qquad (3)$$

Since the output response is the same for both circuits, it is:

$$i'_n = i_n - i_p \qquad (4)$$

where i_{C_M} is the current through the coupling capacitance between input and output.

Initially (after the nMOS transistor starts conducting), the pMOS transistor operates in the linear region (since its V_{DS} is small) and the nMOS transistor in saturation (since its V_{DS} is large). Thus, eq. (4) can be written as :

$$P_{s_n}\frac{W_x}{L}\left(V_{in}-V_{TN}\right)^{a_n} = P_{s_n}\frac{W_n}{L}\left(V_{in}-V_{TN}\right)^{a_n} - P_{l_p}\frac{W_p}{L}\left(V_{DD}-V_{in}-\left|V_{TP}\right|\right)^{a_p/2}\left(V_{DD}-V_{out}\right) \qquad (5)$$

from which the required width of the equivalent transistor W_x can be found as a function of time t and V_{out}.

However, it has been observed that the time point at which the short-circuiting transistor (in this case the pMOS) enters saturation, t_{s_p}, (Fig. 2) is related to the time point when the pMOS transistor ceases to conduct (t_p) by the equation $t_{s_p} = h \cdot t_p$ [9]. The empirical coefficient h depends on the quantity $G_{np} = \frac{\left(I_{DO_n} - 0.2 I_{DO_p}\right)\cdot\tau}{V_{DD} C_L}$ which is a measure of the transconductance of the discharging path and determines how fast the output discharges. G_{np} depends on the drivability of the nMOS and pMOS devices (taking into account the fact that the short-circuit current is much smaller than the driving

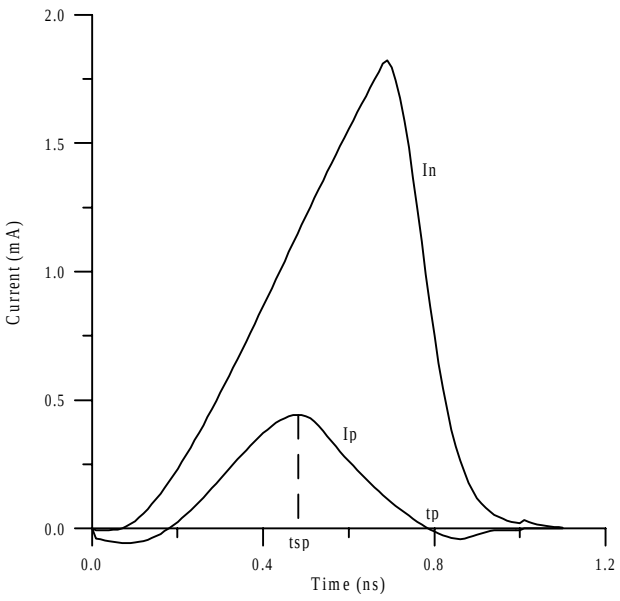


Fig. 2: nMOS and pMOS currents during output transition

Table I: Estimation of empirical parameter *h*

G_{np}	0.2 - 2.5	2.5 - 10	> 10
h	0.65	0.6	0.55

current). $I_{DO_{n/p}}$ is the transistor drain current when $V_{GS} = V_{DS} = V_{DD}$. G_{np} takes also into account the input waveform slope and the output load. In Table I the values of h depending on G_{np} are given for a 0.5 μm HP technology. This approximation has been tested on several inverter configurations and is also validated by the overall results.

Since t_{s_p} is known, the output voltage value at this time point can be calculated because at this point the values of the short-circuit currents in the linear region and in saturation become equal. Consequently :

$$k_{l_p}\left(V_{DD}-V_{in}\left[t_{s_p}\right]-\left|V_{TP}\right|\right)^{a_p/2}\left(V_{DD}-V_{out}\right) = k_{s_p}\left(V_{DD}-V_{in}\left[t_{s_p}\right]-\left|V_{TP}\right|\right)^{a_p} \qquad (6)$$

from which the output voltage at t_{s_p} is easily obtained.

The required value of W_x up to time point t_{s_p} can be found by substituting into eq. (5) the value of V_{out} at t_{s_p}. This value of W_x will be referred to as W_1.

The next region for which the width of the single equivalent transistor should be calculated, is up to time point t_p, since from t_{s_p} to t_p the pMOS transistor operates in saturation. Obviously, at time point t_p the calculated value of W_x would be equal to the nMOS transistor width of the actual inverter since there is no

short-circuit current at this point. Hence, the value of W_x in this region is selected as an average, $W_2 = \frac{W_1 + W_n}{2}$.

In the last region ($t > t_p$), W_x (W_3) is equal to W_n as no short-circuit current exists.

These three distinct W_x values can be used in order to solve the differential equation that describes the operation of the single equivalent transistor in Fig. 1b. Region crossings are determined by the width values, the time point at which the nMOS transistor exits saturation and the time point when the input reaches its final value. Since the form of the differential equation (3) is simpler than that of the initial inverter, the solution and the resulting expressions for the output waveform are simpler and less time consuming. Moreover, for the solution of the differential equation no further approximations are required.

The solution of differential equation (3) in the general case is of the form :

$$V_{out_1}[t] = k_1 - k_2\left[\frac{V_{DD}}{\tau}t - V_{TN}\right]^{a_n+1} + C_1 \qquad (7)$$

when the nMOS transistor operates in saturation and

$$V_{out_2}[t] = C_2 \cdot e^{-k_3\left(\frac{V_{DD}}{\tau}t - V_{TN}\right)^{1+\frac{a_n}{2}}} \qquad (8)$$

when the nMOS transistor operates in the linear region, where

$$k_1 = \frac{C_M V_{DD}}{(C_L + C_M)\tau}, \qquad k_2 = \frac{P_{s_n}\frac{W_x}{L}\tau}{(C_L + C_M)(1+a_n)V_{DD}},$$

$$k_3 = \frac{2P_{l_n}\frac{W_x}{L}\tau}{(C_L + C_M)(2+a_n)V_{DD}}$$ and C_1, C_2 are the integration constants.

For the case of a falling input ramp the estimation of W_x is performed in a symmetrical way.

3. RESULTS AND CONCLUSIONS

Results of the proposed method are given in Fig. 3 where the output waveform of an inverter and that of its equivalent single transistor primitive are plotted for a 0.5 μm (W_n=4μm, W_p=6μm, C_L=100fF) and a 0.35 μm (W_n=2.8μm, W_p=4.2μm, C_L=100fF) HP technology for two different input transition times. The accuracy of the proposed method is obvious.

In order to model CMOS circuits, methods have been developed [1], [3] for collapsing a complex CMOS gate to an equivalent NAND/NOR gate and then to reduce such a gate to an equivalent inverter. This modeling process could be further enhanced employing the proposed method to map an inverter to a single transistor primitive. Such a process is diagrammatically shown in Fig. 4 and simplifies significantly the simulation of large circuits.

Macromodeling can be defined as the process of reformulating the mathematical description (model) of a system in a simpler and thus more tractable way. In this context the proposed macromodel simplifies the transient analysis of a CMOS inverter (and for the general case of a complex CMOS gate) speeding up timing analysis of integrated circuits.

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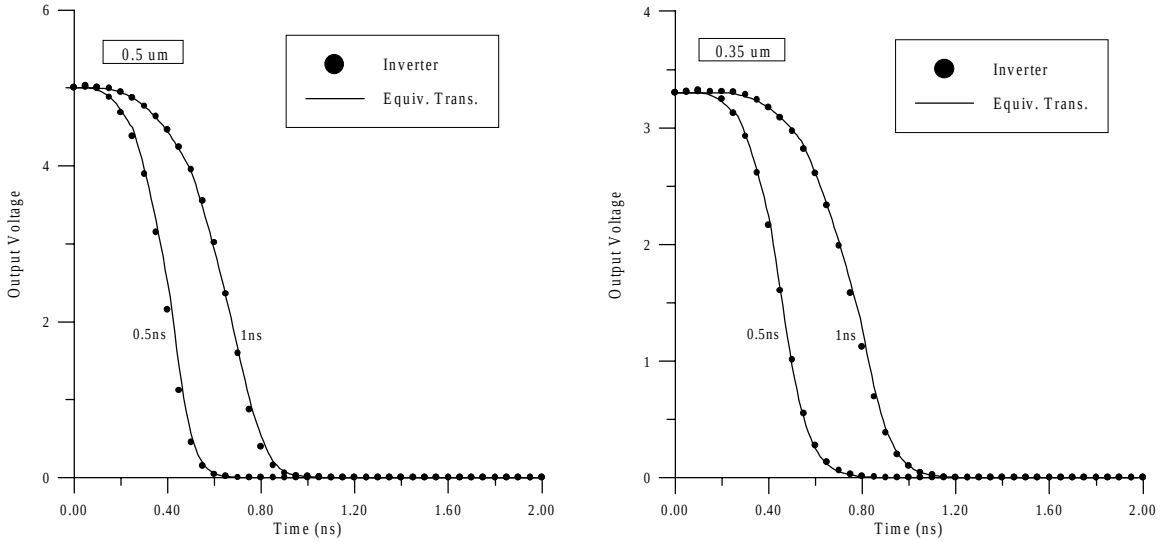

Fig. 3: Output waveform of the CMOS inverter and the single equivalent transistor for two submicron technologies. The input transition time to which each output corresponds is also shown.

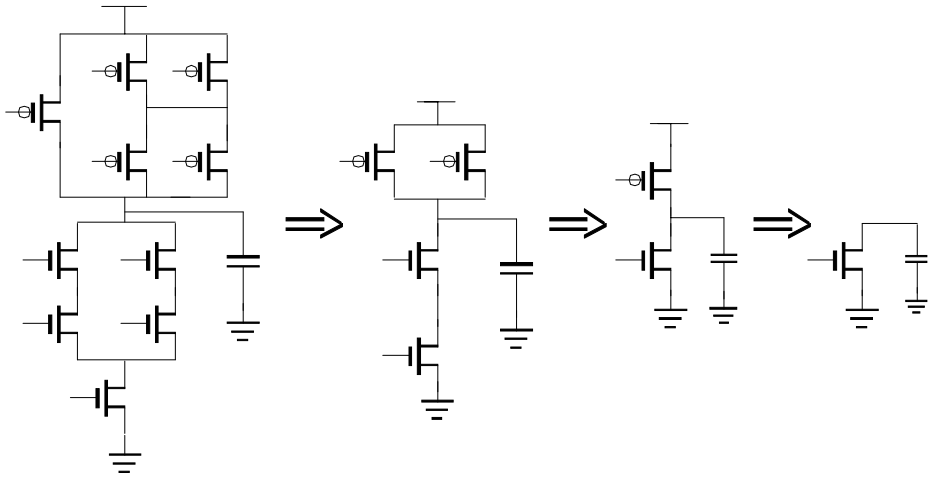

Fig. 4: Mapping process for modeling of CMOS gates