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COLLAPSING THE CMOS TRANSISTOR CHAIN TO AN EFFECTIVE SINGLE EQUIVALENT TRANSISTOR

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Short title : Collapsing the transistor chain to a single transistor

ABSTRACT

A method for collapsing the transistor chain of CMOS gates to a single equivalent transistor is introduced. The width of the equivalent transistor is calculated taking into account the operating conditions of each transistor in the structure, resulting in very good agreement with SPICE simulations. Second order effects such as carrier velocity saturation in submicron devices, body effect and coupling capacitance are considered and ramp inputs are used. The actual time point when the chain starts conducting which influences significantly the accuracy of the model is also extracted. Finally, an algorithm to collapse every possible input pattern to a single input is introduced.

1. INTRODUCTION

The development of digital integrated circuits with short design cycles requires accurate and fast timing simulation. Unfortunately, simulators such as SPICE are excessively slow for large designs. The need for analytical methods which can produce accurate results at short times is obvious and extended research has been conducted, especially for the modelling of the CMOS inverter [1], [2], [3]. More complicated gates such as NAND/NOR structures are difficult to model, mainly because of the multinodal circuitry and multiple inputs of the transistor chain.

Conventionally, the transistor chain is modelled by a single transistor with reduced transconductance according to the number of the transistors in the chain. Several attempts have also been made in order to model the transistor chain trying to exploit the fact that all transistors in the chain except for the top one, operate always in linear mode [4]-[8]. All previous works used simplifying assumptions for the operation of the chain, such as step inputs, resistive behaviour, long channel models and negligible body effect, thus resulting in insufficient accuracy. However, it is often advantageous to model the transistor chain by a single equivalent transistor, since this model can be easily applied in the analysis of more complex gates. In addition, since modelling of parallel transistors can be performed with good accuracy as in [9], the well defined modelling analysis of the inverter can be used.

Nabavi-Lishi and Rumin [10] presented a semi-empirical method for collapsing a transistor chain to a single equivalent transistor following the conventional $(n+1)$-times transconductance reduction for an $(n+1)$ transistor chain, resulting in limited accuracy. In [9] and [10] a way of collapsing multiple inputs to a single one is described, but the extracted waveform leads to large errors, especially when transition times and starting points of some signals differ significantly.

Some of the secondary effects which are present in the operation of the transistor chain have been mentioned in [11], [12], where a chain collapsing technique based on a nonlinear macromodel is proposed, but it extracts parameters from dc analyses and applies them on transient phenomena. Moreover, a simplified theoretical analysis is used for the validation of the proposed effective transconductance model.

In this paper the width of the single equivalent transistor is calculated taking into account the mode of operation of the transistors in the chain. Moreover, the time at which the chain starts conducting is obtained overcoming a main source of errors in all existing modelling techniques. Finally, an input mapping algorithm is presented which leads to a single input signal which effectively replaces all inputs of the chain.

2. TRANSISTOR CHAIN OPERATION

Let us consider the discharging of an output load by the nMOS transistor chain shown in Fig. 1a. The case of a PMOS charging chain is symmetrical. A common rising input ramp is applied to all transistor gates:

$$V_{in} = \begin{cases} 0\,, & t \le 0 \\ \dfrac{V_{DD}}{\tau} \cdot t\,, & 0 < t \le \tau \\ V_{DD}\,, & t > \tau \end{cases} \tag{1}$$

where τ is the input rise time.

The a-power model proposed in [3] which takes into account the carrier velocity saturation effect of short channel devices, is used for the transistor currents :

$$I_D = \begin{cases} 0 & V_{GS} \le V_{TN} \ : \textit{cutoff region} \\ k_l \left(V_{GS} - V_{TN}\right)^{a/2} V_{DS} & V_{DS} < V_{D-SAT} \ : \textit{linear region} \\ k_s \left(V_{GS} - V_{TN}\right)^{a} & V_{DS} \ge V_{D-SAT} \ : \textit{saturation region} \end{cases} \tag{2}$$

where $V_{D\text{-}SAT}$ is the drain saturation voltage, k_l , k_s are transconductance parameters which depend on the width to length ratio of a transistor (e.g. $k_l = P_l \dfrac{W}{L}$), a is the velocity saturation index and V_{TN} is the threshold voltage which is expressed by its first order Taylor series approximation around V_{SB}=1V with very good accuracy as :

$$\widetilde{V}_{TN} = V_{TN}\big|_{V_{SB}=1} + \left(V_{TN}\right)'\Big|_{V_{SB}=1} \cdot \left(V_{SB} - 1\right) = \theta + \delta V_{SB} \tag{3}$$

The above model is much more accurate than Shockley's square law conventional model for short-channel devices, since their actual drain current in the saturation region does not show square law dependence on gate-to-source voltage and the drain saturation voltage is shifted compared to that predicted by Shockley's model. Both discrepancies originate from the velocity saturation effect which is captured by the introduced velocity saturation index α (α<2).

During the evolution of the load discharging, the topmost transistor in the chain (M_{n+1}) operates initially in saturation and then enters the linear region when its $V_{DS}=V_{D\text{-}SAT}$. All other transistors in the chain operate in linear region without ever leaving this region [5]. For the time interval during which the topmost transistor is in saturation and the input is rising, its current and consequently the voltages at the internal nodes are increasing. When the input reaches V_{DD} and until the topmost transistor exits saturation, its current and therefore the internal node voltages remain constant. Thus, the parasitic currents are eliminated and the same current flows through all transistors in the chain. This time period which is known as the "plateau" state [4], is apparent for fast inputs (Fig. 2). An input is considered fast (slow) when the top transistor exits saturation after (before) the input reaches V_{DD}.

In order to calculate the plateau voltage the nonsaturated devices are replaced by an equivalent transistor ($M_{b_{eq}}$) whose width is approximated by :

$$\frac{1}{W_{b_{eq}}} = \frac{1}{W_1} + \frac{1}{W_2} + \ldots + \frac{1}{W_n} \tag{4}$$

The two-transistor equivalent circuit is shown in Fig. 1b. The plateau voltage occurs at the end of the input ramp at time t=τ. The small voltage overshoot which occurs due to coupling capacitances, does not have any significant effect. Equating the currents of the saturated top transistor (M_u) and the bottom transistor ($M_{b_{eq}}$) which operates in linear mode for V_{in}=V_{DD} results in :

$$P_s \frac{W_u}{L}\left(V_{DD} - \theta - (1+\delta)V_p\right)^a = P_l \frac{W_{b_{eq}}}{L}\left(V_{DD} - V_{TO}\right)^{a/2} V_p \tag{5}$$

The value of the plateau voltage is obtained with very good accuracy, using a second order Taylor series approximation for the left-hand side of the equation around V_p=1V.

In the following analysis the source voltage of the top transistor in the chain, V_M, is considered linear for the interval between time t_1, where the chain starts conducting and time τ (fast inputs) or time t_2 (slow inputs) where the top transistor exits saturation. This observation is based on SPICE simulations and leads to highly accurate results. Time points t_1, t_2 are calculated in Appendices A and B respectively. Since time t_1 and $V_M[t_1]$ are known (see Appendix A) and for fast inputs the plateau voltage occurs at time τ, the slope of V_M is also known. For slow inputs the slope of V_M can be calculated in a similar way. Although for slow inputs the plateau voltage is not present, it has been found that if in a chain which receives a slow input the output load is increased, the slope of V_M remains almost the same (Fig. 3). Therefore, considering a sufficiently larger load capacitance, the input would become fast, V_p would occur at time t=τ and would be calculated as previously by eq. (5). Since the slope remains unchanged, the calculated slope is valid for the initial load as well. The independence of V_p on the load capacitance which is required in order for the previous proposition to be valid, is obvious from eq. (5).

3. EFFECTIVE WIDTH OF THE EQUIVALENT TRANSISTOR

In the following analysis all internal nodes of the chain are considered to be discharged at time t=0. In case some of the internal nodes are initially charged, the output waveform should be appropriately shifted, since the trapped charges in the internal nodes cause an additional delay in the output response [4].

It is obvious that a single equivalent transistor will have the same output response with the complete chain, if it successfully manages to reproduce the combined behaviour of the nonsaturated devices with the dual operation of the top transistor, in saturation and the linear region. For the time interval where the top transistor in the chain is saturated, the current through that transistor is the bottleneck for the current that is flowing through the chain [5]. Therefore, in order to obtain the width (W_{eq}) of the single equivalent transistor (M_{eq}) the currents through transistor M_{n+1} of the complete chain and transistor M_{eq} should be set equal :

$$I_{M_{n+1}} = I_{M_{eq}} \Rightarrow P_s \frac{W_{n+1}}{L}\left(V_{in} - \theta - (1+\delta)\, V_M\right)^a = P_s \frac{W_{eq}}{L}\left(V_{in} - V_{TO}\right)^a \qquad (6)$$

The above equation can be solved for several values of t yielding corresponding W_{eq} values. For the time interval [t_1, t_2], W_{eq} plotted against time has the form of Fig. 4. An average value of W_{eq} should be calculated from eq. (6) as the integral of its expression from time t_1 to t_2 over t_2-t_1. However, for simplicity, W_{eq} can be calculated at time $t = \frac{t_1 + t_2}{2}$ with a maximum error 5 %. This value of W_{eq} will be referred to as W_{sat}.

On the other hand, when all transistors in the chain operate in the linear region the transistor chain is considered as a voltage divider and $V_{out} = (n+1) \cdot V_1$ (assuming equal transistor widths). The width of the equivalent transistor can be calculated by equating the currents through transistor M_1 of the chain and transistor M_{eq} :

$$I_{M_1} = I_{M_{eq}} \Rightarrow P_l \frac{W_1}{L}\left(V_{in} - V_{TO}\right)^{a/2} V_1 = P_l \frac{W_{eq}}{L}\left(V_{in} - V_{TO}\right)^{a/2} V_{out} \qquad (7)$$

resulting in $W_{eq} = \frac{W_1}{n+1}$. This value of W_{eq}, which will be referred to as W_{lin}, in contrast to W_{sat}, is constant throughout this region of operation.

As it is observed from SPICE simulations, the drain-to-source voltage of a transistor as we move further up in the chain increases almost linearly. That is because in order for the currents of the transistors in the chain to be equal, the reduction in V_{GS} and the increase in V_{TN} of a transistor closer to the output is compensated by an increase in its V_{DS}. However, this increment factor is very close to unity so that the previously used approximation ($V_{out} = (n+1) \cdot V_1$) proves to be simple and very efficient.

Since the transistor width for each operating condition is known, the chain can be modelled by a single equivalent transistor (Fig. 1c) whose width from time t_1 to time t_2 is W_{sat} and for the rest of the time equal to W_{lin}. A comparison of the complete chain output response with the nonlinear equivalent transistor where two distinct equivalent widths are used according to the region of operation is presented in Fig. 5. The error that is present in the tail of the output response is due to the fact that for the calculation of W_{lin}, the drain-to-source voltage of the bottom transistor in the chain was calculated without taking into account the increment factor mentioned before. This leads to an increased value of W_{lin} and consequently the current through the equivalent transistor in the linear region is larger than the actual and the discharging of the output load is faster.

However, since the aim was to provide an equivalent width that would match the existing inverter models, the above two width values should be efficiently merged into one. This can be accomplished by calculating the fraction of charge (Q_{sat}) that is discharged to ground during the time in which the top transistor in the chain operates in saturation over the total charge ($Q_{total} = C_L V_{DD}$) that is stored initially in the output load and has to be discharged. The current through transistor M_{n+1} can be integrated from time t_1 to time t_2 in order to obtain the charge Q_{sat} :

$$Q_{sat} = \int_{t_1}^{t_2} k_s \left(V_{in} - \theta - (1+\delta)\,\mathrm{V_M}\right)^a dt \tag{8}$$

A saturation coefficient c_{sat} can now be calculated as :

$$c_{sat} = \frac{Q_{sat}}{Q_{total}} \tag{9}$$

Consequently, the corresponding coefficient when all transistors operate in linear mode, is equal to c_{lin}=1-c_{sat}.

Since the calculated coefficients act as the "weight" of each mode of operation on the overall output voltage temporal evolution, the width of the single equivalent transistor can be calculated as :

$$W_{eq} = c_{sat} \cdot W_{sat} + c_{lin} \cdot W_{lin} \tag{10}$$

The time point when the chain starts conducting (t_1) is crucial and in order to obtain accurate results, it should be taken into account. The output waveform of the complete chain is compared to that of the proposed equivalent transistor and the conventional approach with and without calculation of the starting point t_1 and is shown in Fig. 6 for two different transistor chains. In Fig. 7 the error (%) of the three approaches at half-V_{DD} point of the output waveform of the complete chain is presented. The superiority of the proposed method is obvious.

It should be mentioned that when the transistor chain has a parasitic behaviour in the gate operation, e.g. in case of charging the output of a NAND gate, all transistors operate for most of the time in the linear region and a reasonable model for the chain is an equivalent transistor with width $W_{eq} = \dfrac{W}{n+1}$. However, the coupling capacitance between inputs and the internal nodes of the chain has a non negligible effect on the output response. Adding between the input terminal of the equivalent transistor and its drain node the lumped capacitance of all gate-to-drain and gate-to-source capacitances in the chain, as it is calculated using the Elmore delay formula, increases the accuracy significantly.

4. SINGLE EFFECTIVE INPUT EXTRACTION

Definitions: n+1 input ramps which are applied to the n+1 transistors of a chain and have the same transition time and starting time, will be referred to as *normalized inputs* and the single equivalent one as *normalized input*. Additionally, every set of input ramps (less than n+1) which have the same transition time and the same starting point, will be referred to as *equal ramps.*

The proposed algorithm aims to the extraction of n+1 normalized input ramps for each possible input pattern consisting of ramps and dc voltages, so that when the normalized inputs are applied, the chain will have the same output response with that of the actual inputs. Before the proposed algorithm can be applied, the "weight" of each transistor in the chain has to be calculated, i.e. a coefficient which corresponds to the position of each input (or combination of inputs). Equal ramps are applied to the gates of the transistors for which the weight coefficients are to be calculated and all other inputs are set to V_{DD}. For each case of input patterns, a coefficient is derived with whom the transition time of the applied ramp must be multiplied so that when the resulted ramp is applied to all transistors, the evolution of the output will be the same. These coefficients have been found to be almost independent of the transistor width and the input transition time and the extracted coefficients for a 4-transistor chain are presented in Table I. It should be mentioned that non-simultaneous inputs might create a conducting path from the output to some internal nodes. The effect of the introduced charges on the output evolution is incorporated in the calculation of the weight coefficients.

The next three steps of the mapping algorithm should be applied for every possible input pattern :

Step 1. Inputs which efficiently act and should be treated as V_{DD} voltages have to be identified. In order to achieve this, every input ramp which at time $t=t_m$ has a value larger than $\frac{2}{3}V_{DD}$ should be considered V_{DD} for the following steps. Time t_m occurs when the last ending input ramp reaches $V_{DD}/2$. In case two or more inputs end at the same time, t_m is measured on the one that starts last.

Step 2. The m ramp inputs that remain from step 1 have to be transformed to equal ramps. The starting point of these equal ramps (t_0) is taken as t_0=max(t_1, t_2, ..., t_{n+1}) where t_1, t_2, ..., t_{n+1} are the starting point of **all** input ramps in the chain. In order to take into account the slope and the time during which an input is in transition after time t_0, the transition time (T_{eq}) of the equal ramps is taken as :

$$T_{eq} = \frac{\sum_{i=1}^{m}\left[1-\frac{V_i[t_0]}{V_{DD}}\right]\left(t_{e_i}-t_0\right)}{m} \tag{11}$$

where $V_i[t_0]$ is the voltage that each input ramp has reached at the initial time and t_{e_i} is the time point at which each of the m input ramps reaches V_{DD}.

Step 3. The input pattern which is now applied to the chain, consists of equal ramp inputs and V_{DD} inputs. These can be mapped to normalized inputs using the weight coefficients which correspond to the positions of the switching transistors in the chain. Thus, the transition time of the resulted normalized inputs which are applied to the chain at time $t=t_0$ is :

$$T_{eff} = c_{weight} \cdot T_{eq} \tag{12}$$

The same ramp (normalized input) is finally applied to the single equivalent transistor.

In Fig. 8, a comparison of the output responses of a five transistor chain to the actual and normalized input patterns is presented, which shows the accuracy of the proposed algorithm.

5. CONCLUSION

A very efficient method for collapsing a transistor chain to a single equivalent transistor has been introduced. The width of the equivalent transistor is calculated taking into account the operating conditions of the structure. Parameters such as the time when the chain starts conducting, short channel current expressions, ramp inputs and the influence of body effect have been incorporated in the model. In addition, an efficient and accurate algorithm has been proposed in order to extract a single equivalent input from every possible input pattern to a chain.

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APPENDIX A

Since each transistor in the chain has a different source and threshold voltage, the time at which the condition $V_{GS} - V_{TN} = 0$ for each one is satisfied and the transistor starts conducting is also different. Coupling capacitance between the transistor gates and the drain/source nodes forces each internal node voltage to follow the input ramp until all transistors below that node start conducting. From this point on, the node voltage is also subject to another opposite trend due to the current flowing to ground and tends to pull the node voltage down. In order to obtain time t_1, when the chain starts conducting, it is assumed that these two trends are counterbalanced (Fig. 9), thus leading in a constant node voltage until time t_1.

The waveform of the node voltages until the transistors below the *i*-th node start conducting at time t_{s_i} can be found by equating the current through the coupling capacitance $\left(I_{C_{M_i}}\right)$ with the charging current of the parasitic node capacitance I_{C_i} :

$$I_{C_{M_i}} = I_{C_i} \Rightarrow C_{M_i} \frac{dV_{in} - dV_i}{dt} = C_i \frac{dV_i}{dt} \Rightarrow V_i\left[t\right] = \frac{C_{M_i}}{C_{M_i} + C_i} V_{in}\left[t\right] \tag{13}$$

where C_{M_i} is calculated as the sum of the gate-to-source and gate-to-drain overlap capacitances of the upper and lower transistors respectively and C_i is calculated as a function of "base" area and "sidewall" periphery of the node junction according to [13].

The time at which the *i*-th transistor starts conducting can be calculated recursively by solving :

$$V_{GS_i}\left[t_{s_i}\right] - V_{TN_i}\left[t_{s_i}\right] = 0 \Rightarrow V_{in}\left[t_{s_i}\right] - V_{i-1}\left[t_{s_{i-1}}\right] - \left(\theta + \delta \cdot V_{i-1}\left[t_{s_{i-1}}\right]\right) = 0 \tag{14}$$

which leads to :

$$t_{s_i} = \tau \frac{\theta + (1+\delta)\dfrac{C_{M_{i-1}}}{C_{M_{i-1}} + C_{i-1}} \dfrac{V_{DD}}{\tau} t_{s_{i-1}}}{V_{DD}} \tag{15}$$

where i corresponds to the position of the transistor in the chain ($t_{s_0} = 0$). The time at which the chain turns on is calculated using the above expression, as $t_1 = t_{s_{n+1}}$. A comparison between the calculated time point t_1 with the actual one is presented in Fig. 10.

APPENDIX B

In order to obtain the time point (t_2) at which the top transistor in the chain exits saturation, the output voltage expression has to be found by solving the following differential equation at the output node :

$$C_L \frac{dV_{out}}{dt} = -k_s \left(V_{in} - \theta - (1+\delta)V_M\right)^a \tag{16}$$

For slow inputs the solution is :

$$V_{o_s} = \left(k_1 t - k_2\right)^a \frac{k_s}{C_L k_1 (1+a)} \left(k_2 - k_1 t\right) + C[1] \tag{17}$$

where $V_M = m_1 + m_2 t$, $m_1 = V_M\left[t_1\right] - m_2 t_1$, $m_2 = \dfrac{V_p - V_M\left[t_1\right]}{\tau - t_1}$ ($V_M[t_1]$ is known from appendix A), $k_1 = s - (1+\delta)m_2$, $k_2 = \theta + (1+\delta)m_1$, $s = \dfrac{V_{DD}}{\tau}$ and C[1] is found by setting $V_{o_s}\left[t_1\right] = V_{DD}$. For fast inputs :

$$V_{o_f} = -\frac{k_s \left(V_{DD} - \theta - (1+\delta)V_p\right)^a}{C_L} t + C[2] \tag{18}$$

where C[2] is found by setting $V_{o_f}[\tau] = V_{o_s}[\tau]$.

Time t_2 is calculated by equating the drain saturation voltage with the actual drain-to-source voltage of transistor M_{n+1} :

$$V_{D-SAT}\left[t_2\right] = V_{out}\left[t_2\right] - V_M\left[t_2\right] \tag{19}$$

In order to solve eq. (19) for the case of slow inputs, a first order Taylor series approximation should be used for the term $V_{D-SAT} = \frac{k_s}{k_l}\left(V_{in} - \theta - (1+\delta)\left(m_1 + m_2 t\right)\right)^{a/2}$ [3].

Table I: "Weight" coefficients for a 4-transistor chain. The input numbering starts from the one closest to the ground (L=0.5 μm)

Changing Inputs	c_{weight}
1,2,3,4	1
2,3,4	0.93
1,3,4	0.89
1,2,4	0.85
1,2,3	0.92
3,4	0.82
2,4	0.77
1,4	0.74
2,3	0.815
1,3	0.775
1,2	0.8
4	0.71
3	0.67
2	0.64
1	0.6

LIST OF FIGURE CAPTIONS

Fig. 1: (a) Complete transistor chain, (b) two transistor equivalent circuit and (c) single equivalent transistor model. The parasitic node capacitances are also shown.

Fig. 2: Output and intermediate node voltages of a transistor chain for a fast input ramp

Fig. 3: Intermediate node voltage waveforms for the same input ramp and different output loads

Fig. 4: Single transistor equivalent width for the saturation region

Fig. 5: Output waveform comparison between the complete chain and the nonlinear equivalent transistor for a six transistor chain and τ=3ns

Fig. 6: Output waveforms of the complete chain, the proposed single equivalent transistor and the conventional method with and without t_1 correction, for a (a) four transistor chain, τ=5ns and C_L=50 fF and (b) six transistor chain, τ=3ns and C_L=100 fF

Fig. 7: Percentage error at $V_{DD}/2$ between actual output response and the single equivalent transistor output response for different approaches and for (a) four transistor chain, C_L=50 fF and (b) six transistor chain, C_L=100 fF.

Fig. 8: Actual set of inputs (left column) and normalized equivalent one together with the corresponding output waveform for each case. The dots correspond to the actual set of inputs. The starting point and the transition time of each input ramp is given in ns.

Fig. 9: Simplified representation of intermediate node voltages for a 5-transistor chain

Fig. 10: Comparison between calculated and actual conduction start time point (t_1) for a 4-transistor chain

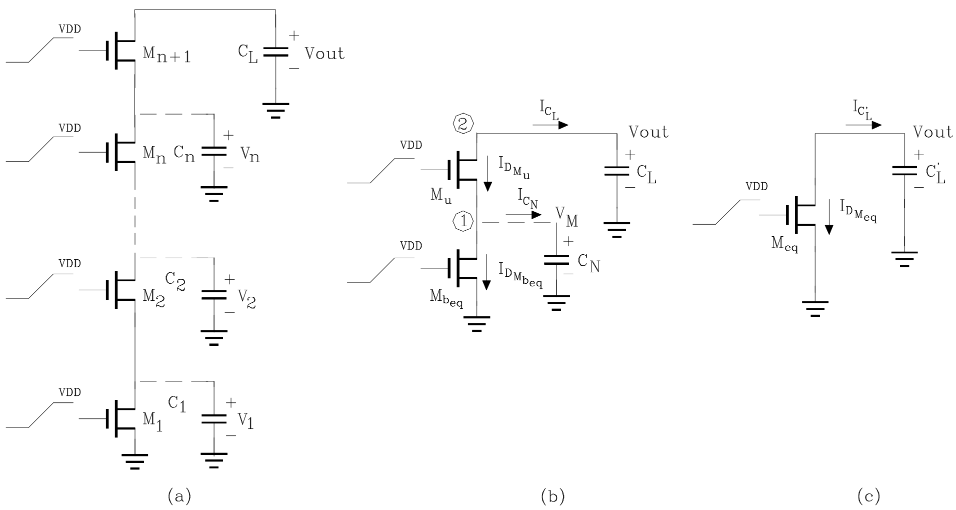


Fig. 1: (a) Complete transistor chain, (b) two transistor equivalent circuit and (c) single equivalent transistor model. The parasitic node capacitances are also shown.

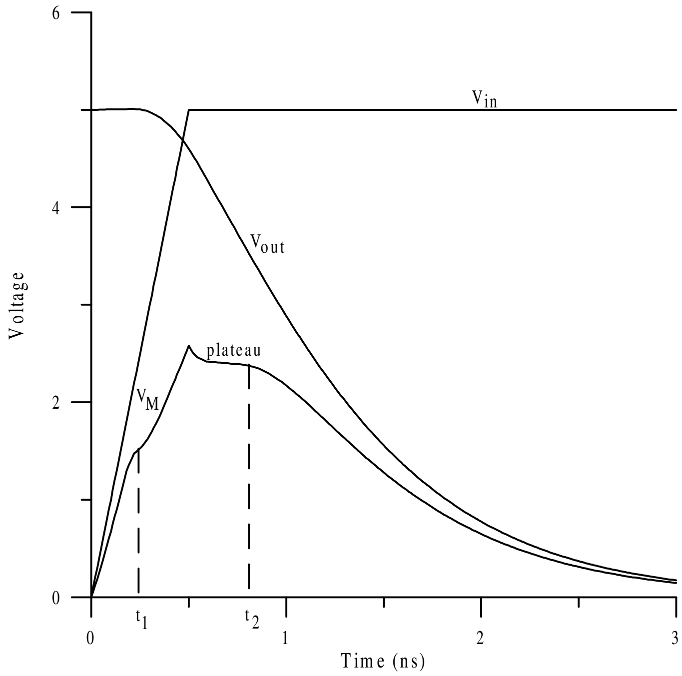


Fig. 2: Output and intermediate node voltages of a transistor chain for a fast input ramp

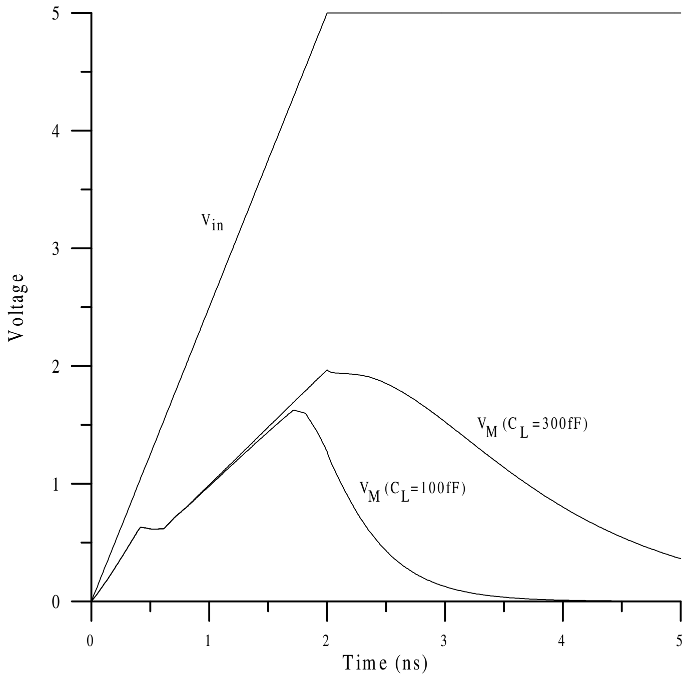


Fig. 3: Intermediate node voltage waveforms for the same input ramp and different output loads

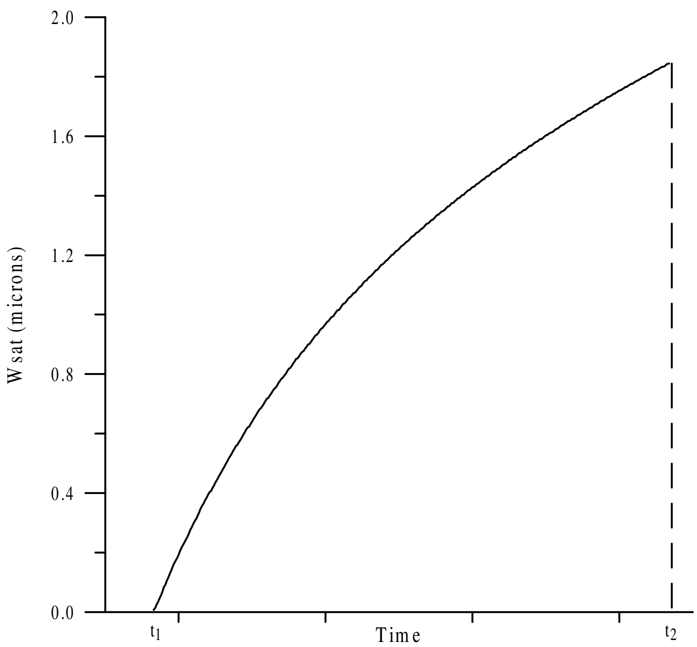


Fig. 4: Single transistor equivalent width for the saturation region

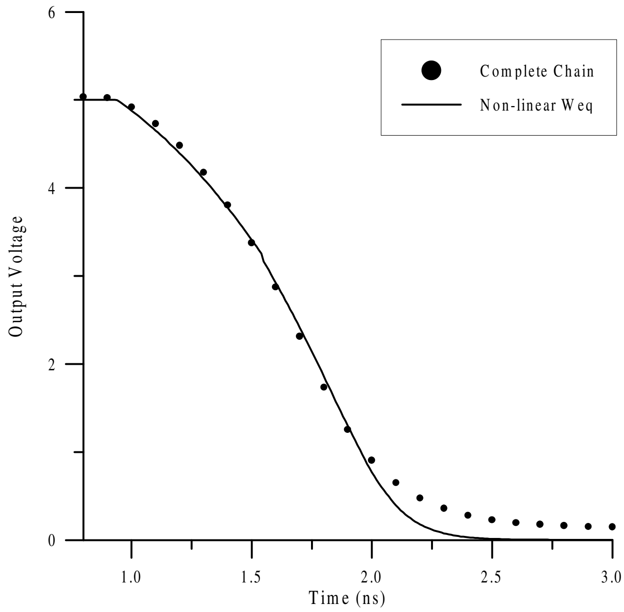
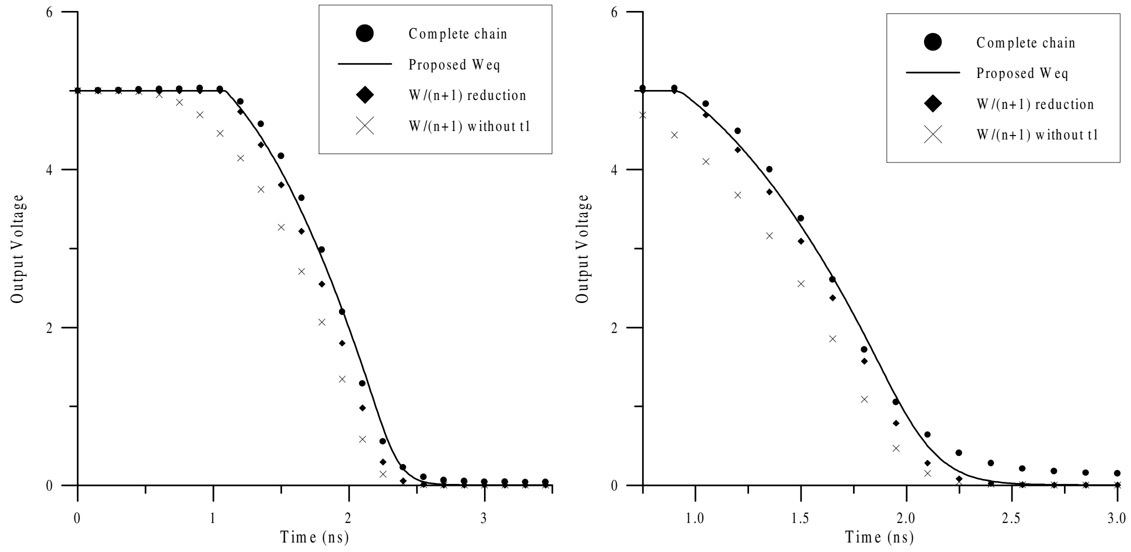
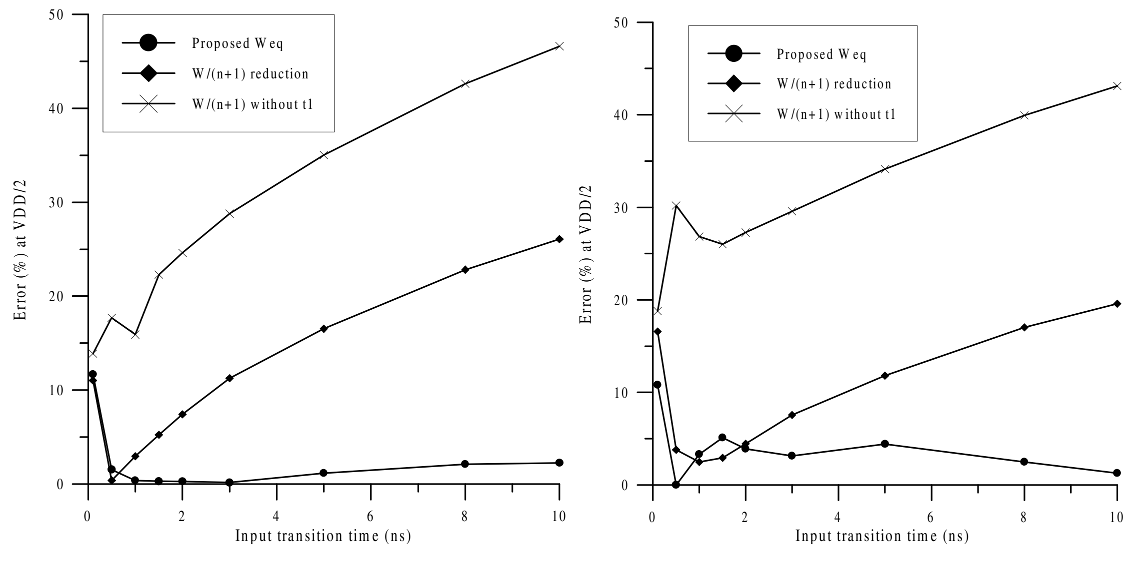


Fig. 5: Output waveform comparison between the complete chain and the nonlinear equivalent transistor for a six transistor chain and τ=3ns



(a) (b)

Fig. 6: Output waveforms of the complete chain, the proposed single equivalent transistor and the conventional method with and without t_1 correction, for a (a) four transistor chain, τ=5ns and C_L=50 fF and (b) six transistor chain, τ=3ns and C_L=100 fF



(a) (b)

Fig. 7: Percentage error at $V_{DD}/2$ between actual output response and the single equivalent transistor output response for different approaches and for (a) four transistor chain, C_L=50 fF and (b) six transistor chain, C_L=100 fF.

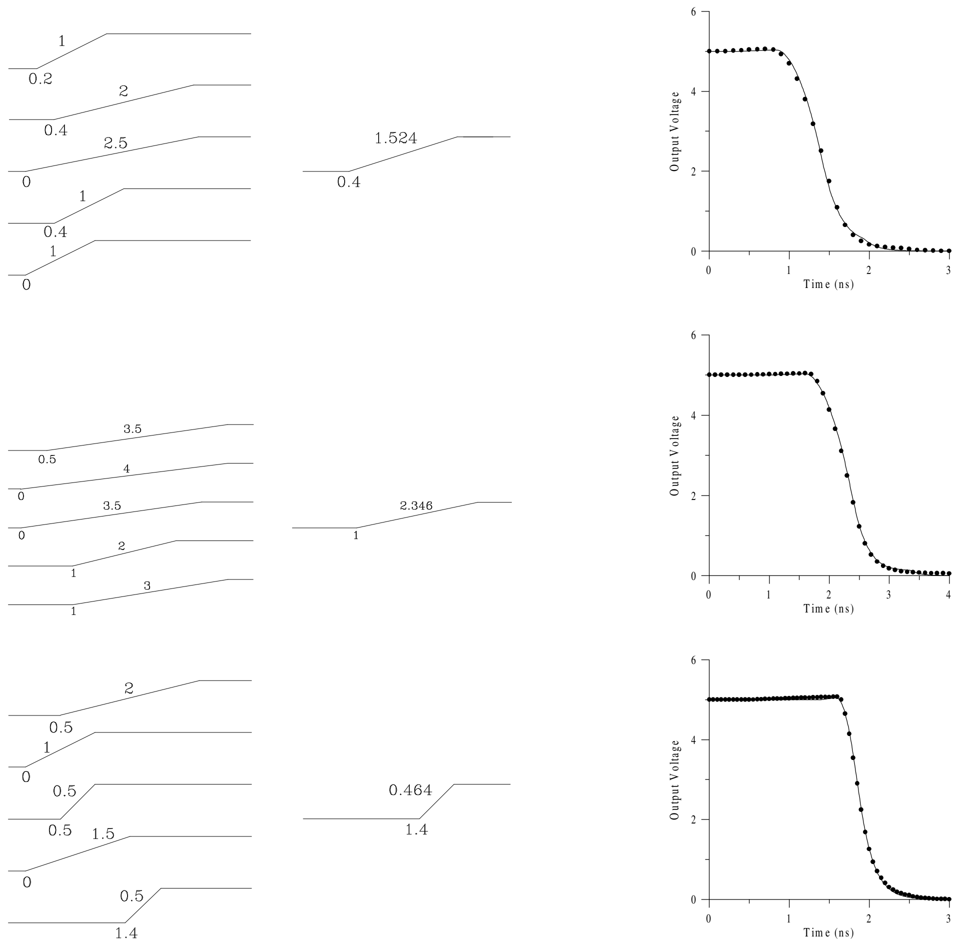


Fig. 8: Actual set of inputs (left column) and normalized equivalent one together with the corresponding output waveform for each case. The dots correspond to the actual set of inputs. The starting point and the transition time of each input ramp is given in ns.

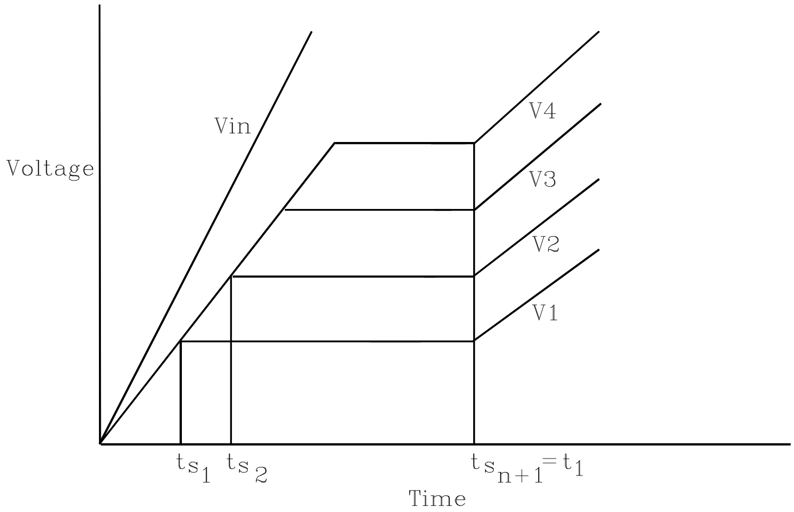


Fig. 9: Simplified representation of intermediate node voltages for a 5-transistor chain

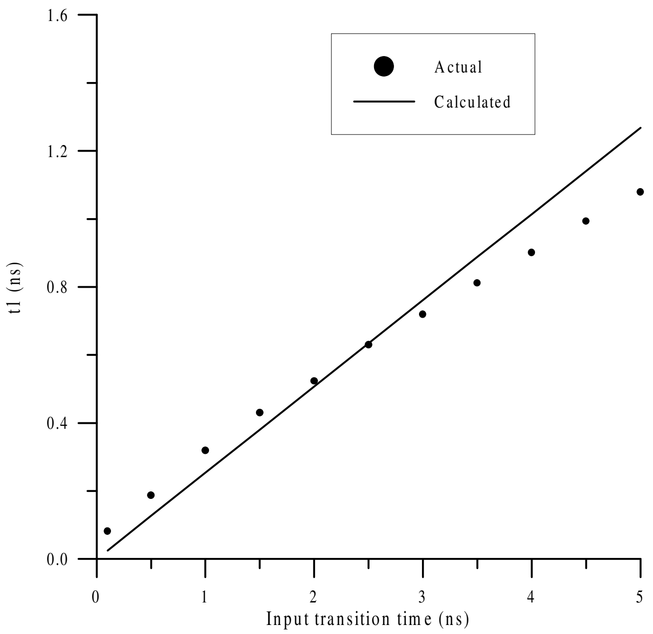


Fig. 10: Comparison between calculated and actual conduction start time point (t_1) for a 4-transistor chain