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INPUT MAPPING ALGORITHM FOR MODELLING OF CMOS CIRCUITS

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ABSTRACT

An algorithm for mapping every possible input pattern of a CMOS gate to an equivalent set of normalized inputs (inputs which have the same starting point and transition time) is presented. Such an algorithm is required in order to perform analytical modelling of CMOS gates and the obtained results are of excellent accuracy compared to SPICE simulations.

I. INTRODUCTION

Analytical methods for modelling of CMOS gates are using ramps as input signals and are based on the assumption that all input ramps applied to a gate have the same transition time and starting point. From this point on, such inputs will be referred to as *normalized inputs*. Normalized inputs are required in order to proceed to the solution of the differential equations which describe the operation of the circuit or to extract a single input that will be applied to an equivalent inverter. However real signals are almost never normalized and an

algorithm is required in order to map these signals to equivalent normalized ramps which are mathematically tractable. Although the problem has been treated for parallel connected transistors [1], the case of serially connected transistors presents higher complexity due to multiple internal nodes and previous attempts [1, 2] introduce large errors.

The influence of each input signal depends on many factors: First of all, the starting point of the last changing input is important, since the transistor chain starts conducting after this time. In addition, the influence of each input depends on the position of the transistor that is applied to, within a transistor chain. Also it depends on its slope, the relation of its slope to the slope of other signals, and its relative position in time to other signals. All these factors are taken into account in the following method.

II. TRANSISTOR POSITION WEIGHT CALCULATION

Let us assume that non-normalized inputs are applied to the n input nMOS transistor chain of Fig. 1. Before the proposed algorithm can be applied, the "weight" of each transistor in the chain has to be calculated, i.e. a coefficient which corresponds to the position of each switching input (or combination of inputs). We define *equal* ramps as any number of normalized ramps less than n. Using only one set of simulations for each technology, these weight coefficients can be obtained as follows : Equal ramp(s) with transition time τ are applied to one or more transistors in the chain whose weight coefficient is to be measured and the rest of the transistors receive a V_{DD} voltage (pattern *CASE*). Then, the amount of charge that is discharged through the chain during input transition is measured. If the same input ramp is applied to all transistors in the chain (pattern

ALL) the rate of discharging slows down and the charge which is discharged in the same time interval will be a fraction of that of pattern *CASE*. Thus, it is :

$$\int_{t_1}^{\tau} I_{all}[t] \cdot dt = g \cdot \int_{t_1}^{\tau} I_{case}[t] \cdot dt \tag{1}$$

where I_{case}, I_{all} are the currents that are flowing through the bottom transistor for the corresponding cases. The fractional coefficient g (g<1) can be easily obtained, with SPICE.

For each case, the aim is to find the corresponding normalized inputs (pattern *NORM*) which start at the same point with the applied equal ramps of pattern *CASE*, but have a different transition time (τ_{norm}), so that the system has the same output response with that of pattern *CASE*. It is obvious that $\tau_{norm}<\tau_{case}$. When two transistor chains have the same output response, the currents of the bottom transistors are equal at each time. Therefore, $I_{case}[t] = I_{norm}[t]$ where I_{norm} is the current through the bottom transistor when the normalized inputs are applied to all transistors in the chain. Integrating both sides of this equation from time $t=t_1$ to τ :

$$\int_{t_1}^{\tau} I_{case}[t]\ dt = \int_{t_1}^{\tau_{norm}} I_{norm}[t]\ dt + \int_{\tau_{norm}}^{\tau} I_{norm}[t]\ dt \tag{2}$$

By equating (1) and (2) and replacing the transistor currents (all transistors except for the topmost operate always in linear mode [3]) with their expressions according to the alpha-power law model [4], it is :

$$\int_{t_1}^{\tau_{norm}} k_l \left(\frac{V_{DD}}{\tau_{norm}} t - V_{TO} \right)^{a/2} \frac{\widetilde{V}_p}{\tau_{norm}} t\ dt + \int_{\tau_{norm}}^{\tau} k_l \left(V_{DD} - V_{TO} \right)^{a/2} \widetilde{V}_p\ dt = \frac{1}{g} \int_{t_1}^{\tau} k_l \left(\frac{V_{DD}}{\tau} t - V_{TO} \right)^{a/2} \frac{\widetilde{V}_p}{\tau} t\ dt \tag{3}$$

For the above equation to be valid, the input should be fast so that during the time interval $\left[\tau_{norm}, \tau\right]$ V_{DS} of the bottom transistor remains constant and equal

to $\widetilde{V}_p = \frac{V_p}{n-1}$ (for non-tapered chains), where V_p is the "plateau" voltage [3]. The above equation can be solved for τ_{norm} and finally the weight coefficient for each case is calculated as :

$$c_{weight} = \frac{\tau_{norm}}{\tau} \tag{4}$$

Although the above calculation is performed for a specific transition time of the inputs the obtained weight coefficients have been found to be valid for a wide range of input transition times. In addition, the calculated coefficients are according to eq. (3), independent of the transistor widths. The "weight" coefficients c_{weight} for a 4-transistor chain are given in Table I for a 0.5 μm HP technology.

III. INPUT MAPPING ALGORITHM

The next three steps of the mapping algorithm should be applied for every possible input pattern (here presented for the case of an nMOS chain) :

Step 1. Inputs which efficiently act and should be treated as V_{DD} voltages have to be identified. In order to achieve this, every input ramp which at time $t=t_m$ has a value larger than $\frac{2}{3}V_{DD}$ should be considered V_{DD} for the following steps. Time t_m occurs when the last ending input ramp reaches $V_{DD}/2$. In case two or more inputs end at the same time, t_m is measured on the one that starts last.

Step 2. The m ramp inputs that remain from step 1 have to be transformed to equal ramps. The starting point of these equal ramps (t_0) is taken as $t_0=\max(t_1, t_2, ..., t_n)$ where $t_1, t_2, ..., t_n$ are the starting point of **all** input ramps in the chain. The transition time (T_{eq}) of the the equal ramps is taken as :

$$T_{eq} = \frac{\sum_{i=1}^{m}\left[1 - \frac{V_i[t_0]}{V_{DD}}\right]\left(t_{e_i} - t_0\right)}{m} \quad (5)$$

where $V_i[t_0]$ is the voltage that each input ramp has reached at the initial time and t_{e_i} is the time point at which each of the m input ramps reaches V_{DD}.

Step 3. The resulted input pattern from step 2 which consists of equal ramps and V_{DD} inputs can be mapped to an equivalent normalized one consisting only of ramp inputs which are applied to the chain at time $t=t_0$ and have a transition time :

$$T_{eff} = c_{weight} \cdot T_{eq} \quad (6)$$

The normalized ramps are finally applied to the transistor chain.

The above algorithm presented very good accuracy for inputs with a wide range of transition times and relative distances in time of their starting points. In Fig. 2, a comparison of the output responses of a four transistor chain to the actual and normalized input patterns is presented. The algorithm can be applied symmetrically in the case of a pMOS transistor chain.

REFERENCES

[1] Y.-H. Jun, K. Jun and S.-B. Park, "An Accurate and Efficient Delay Time Modeling for MOS Logic Circuits Using Polynomial Approximation", IEEE Trans. on Computer-Aided Design, vol. 8, no. 9, pp. 1027-1032, September 1989.

[2] A. Nabavi-Lishi and N. C. Rumin, "Inverter Models of CMOS Gates for Supply Current and Delay Evaluation", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 13, no. 10, pp. 1271-1279, October 1994.

[3] S. M. Kang and H. Y. Chen, "A Global Delay Model for Domino CMOS Circuits with Application to Transistor Sizing", Int. J. Circuit Theory and Applications., vol. 18, pp. 289-306, 1990.

[4] T. Sakurai and A. R. Newton, “Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas”, IEEE J. Solid-State Circuits, vol. 25, no. 2, pp. 584-594, April 1990.

LIST OF CAPTIONS

Table I. : "Weight" coefficients for a 4-transistor chain. The input numbering starts from the one closest to the ground

Fig. 1: nMOS Transistor chain

Fig. 2: Comparison between the output responses of the transistor chain (L=0.5 μm) for actual inputs (dots) and for normalized ones. The starting point and the transition time of each input ramp is given in ns

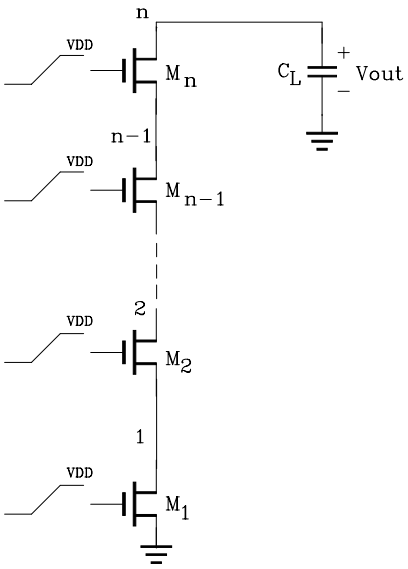

Fig. 1: nMOS Transistor chain

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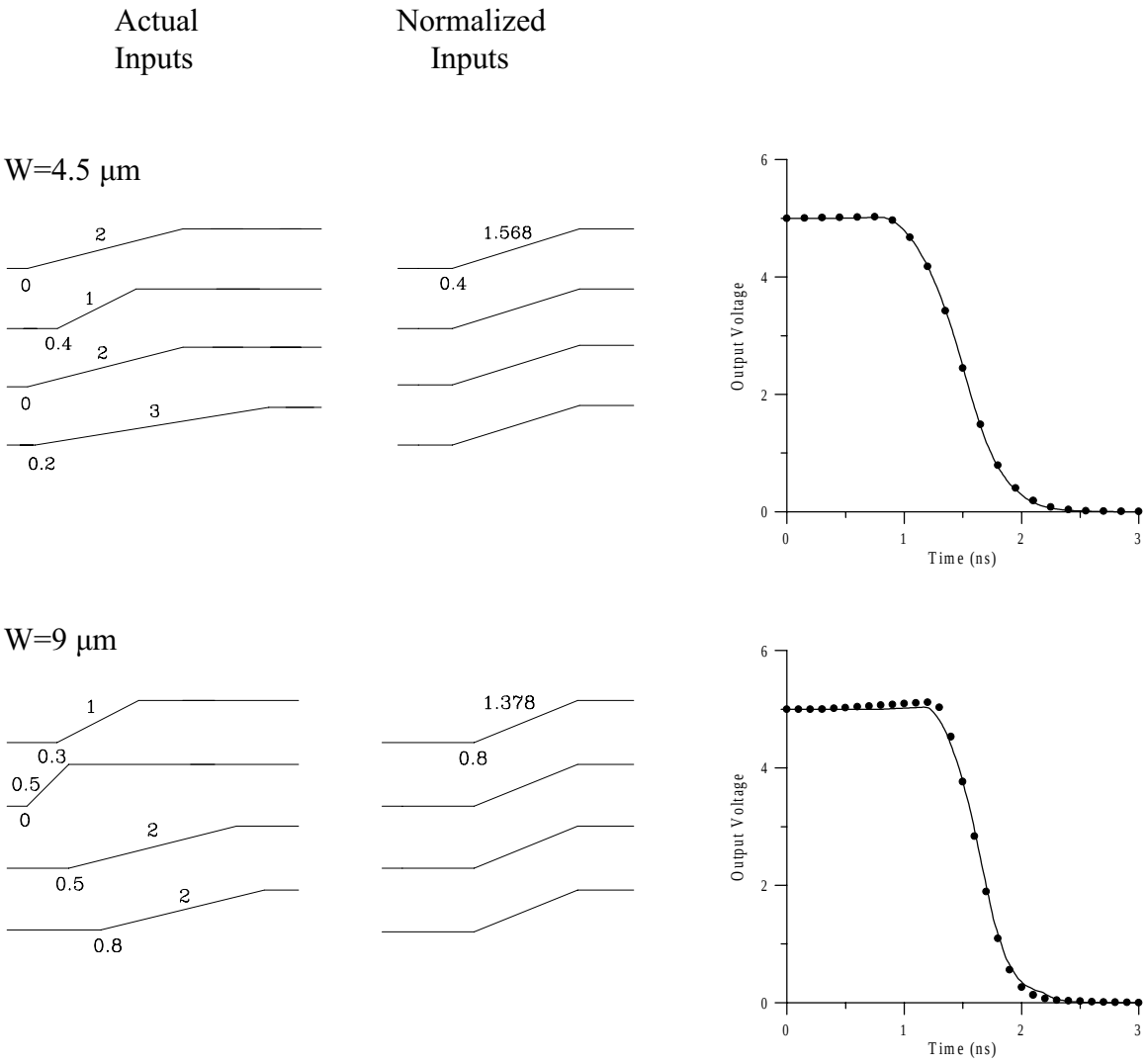
Changing Inputs	c_{weight}
1,2,3,4	1
2,3,4	0.93
1,3,4	0.89
1,2,4	0.85
1,2,3	0.92
3,4	0.82
2,4	0.77
1,4	0.74
2,3	0.815
1,3	0.775
1,2	0.8
4	0.71
3	0.67
2	0.64
1	0.6



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