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ESTIMATING STARTING POINT OF CONDUCTION OF CMOS GATES

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Abstract

In order to model effectively the output waveform and the propagation delay of a CMOS gate, the knowledge of the time point when it starts conducting is essential. An efficient method for calculating analytically this point taking into account the structure of the gate and the input waveform is introduced. Such a method can be easily integrated in a timing analysis system.

I. Introduction

Realistic simulation of digital circuits requires the estimation of the time point when the output node of a gate starts charging/discharging. CMOS gates consist of parallel and serial transistor structures. For the analysis of complex gates, techniques are used for mapping them to equivalent NAND/NOR structures and performing the analysis at this level or they proceed further and reduce the resulted structures to an equivalent inverter [1]. In addition to this transistor structure manipulation, all possible inputs to a gate have to be mapped to an

effective single equivalent ramp [2]. Consequently, in order to develop accurate models of the gate behavior, it is vital to calculate accurately the exact time point when parallel or serial connected transistors, which receive the same input, start conducting.

Parallel transistor structures are trivial to handle, since the starting point of conduction of the parallel group is the same to that of a single transistor (time point when the input becomes equal to the threshold voltage). However, the calculation of the starting point for the serial transistor structure (transistor chain) is more complicated and depends, apart from the input slope and threshold voltage, on the number of the transistors, the parasitic coupling and node capacitances, the body effect, the transistor's drivability and the supply voltage. The effect of all these factors has to be captured by a closed mathematical expression that can be incorporated in existing gate models.

II. Analysis

In a transistor chain with initially discharged internal nodes and the same input ramp (with transition time τ) applied to the gates of all transistors (Fig. 1a), the closer to the output transistors start conducting later because of a gradual increase in their source and threshold voltage. Let us consider the example of a six nMOS transistor chain through which the output load is discharged. The analysis for a pMOS transistor chain is symmetrical. Fig. 2b shows a simplified representation of the actual drain voltages of the five lower transistors shown in Fig. 2a. Because of coupling capacitance between transistor gates and the drain/source nodes, drain voltages tend to follow the input ramp until all lower transistors start conducting. Initially the transistors are in the cut-off region and the coupling

capacitance, C_M, is calculated as the sum of the gate-to-source and gate-to-drain overlap capacitance of the upper and lower transistor respectively, at each node. Until the time when the transistor below the *i*-th node starts conducting, the voltage waveform at that node, $V_i[t]$, as it is isolated between two cut-off transistors, is derived by equating the current due to the coupling capacitance of the node, $I_{C_{M_i}}$, with the charging current of the parasitic node capacitance I_{C_i} :

$$C_{M_i}\frac{dV_{in}-dV_i}{dt}=C_i\frac{dV_i}{dt}\Rightarrow V_i[t]=\frac{C_{M_i}}{C_{M_i}+C_i}V_{in}[t] \quad (1)$$

After the time at which all transistors below the *i*-th node start conducting $\left(t_{s_i}\right)$ and until the time at which the complete chain starts to conduct (t_{on}), this node is subject to two opposite trends. One tends to pull the voltage of the node high and is due to the coupling capacitance between input and the node and is intense for fast inputs and high coupling to node capacitance ratio. The other tends to pull its voltage down because of the discharging currents through all lower transistors and is more intense for nodes closer to the ground.

When a transistor starts to conduct, e.g. transistor #*i*, it operates initially in saturation. Therefore, since its gate-to-drain coupling capacitance is very small, the second (except for the case of very fast inputs where, however, the requirement for accuracy is relaxed since the value of t_{on} remains small) from the above mentioned trends dominates after time t_{s_i} and the voltage at node *i* decreases (Fig. 2). This continues until time $t_{s_{i+1}}$ when transistor #*i*+1 starts conducting and enters saturation. Transistor #*i*, since its V_{GS} continues to increase after time t_{s_i} while its V_{DS} decreases, will enter the linear region close to $t_{s_{i+1}}$. From this point on, the gate-to-source coupling capacitance of transistor #*i*+1

increases by $(2/3)C_{ox}WL$ and the gate-to-drain coupling capacitance of transistor #*i* increases by $(1/2)C_{ox}WL$. Because of this increased coupling capacitance at node #*i*, the two previously mentioned trends are counterbalanced and for simplicity the node voltage is considered constant and equal to its value at $t_{s_{i+1}}$. This observation has also been verified by SPICE simulations (Fig. 2a). The node voltages start to rise again when the complete chain starts conducting at time t_{on}. Additionally, the slope of the voltage waveform during $[t_{s_i}, t_{s_{i+1}}]$ is considered the same for each node and the voltage expression of node 1 during this period can be calculated by solving the differential equation which results from the application of Kirchhoff's current law at node 1 (Fig. 1b) :

$$i_{n_1} = i_{C_{M1}} - i_{C_1} \Rightarrow k_s \cdot \left(V_{in} - V_{TO}\right)^a = C_{M_1}\left(\frac{dV_{in}}{dt} - \frac{dV_1}{dt}\right) - C_1 \frac{dV_1}{dt} \qquad (2)$$

where the transconductance k_s is measured on the I-V_{DS} characteristics and V_{TO} is the zero bias threshold voltage. For simplicity the velocity saturation index α which is imposed by the α-power law model [3], is considered one, which is a reasonable approximation for submicron devices.

Since $t_{s_1} = \frac{V_{TO} \cdot \tau}{V_{DD}}$ is known and $V_1\left[t_{s_1}\right]$ is given by eq. (1), the expression of $V_1[t]$ during $\left[t_{s_1}, t_{s_2}\right]$ is derived and can be used in order to calculate the time, t_{s_2}, when the next transistor further up in the chain starts conducting, by solving $V_{GS_2}\left[t_{s_2}\right] - V_{TN_2}\left[t_{s_2}\right] = 0$. Consequently, the average slope r of each node voltage waveform during $[t_{s_i}, t_{s_{i+1}}]$ can be obtained. In order to incorporate the body

effect in the analysis the threshold voltage is approximated by a first order Taylor series around V_{SB}=1V as $\theta+\delta V_{SB}$, where V_{SB} is the source to substrate voltage.

Finally, the time point at which transistor #*i* in the chain starts conducting can be found by solving :

$$V_{GS_i}\left[t_{s_i}\right]-V_{TN_i}\left[t_{s_i}\right]=V_{in}\left[t_{s_i}\right]-\theta-(1+\delta)V_{i\text{-}1}\left[t_{s_i}\right]=0 \tag{3}$$

where $V_{i-1}\left[t_{s_i}\right]=\dfrac{C_{M_{i-1}}}{C_{M_{i-1}}+C_{i-1}}\cdot V_{in}\left[t_{s_{i-1}}\right]-r\cdot\left(t_{s_i}-t_{s_{i-1}}\right)$

which results in the recursive expression :

$$t_{s_i}=\frac{\theta+(1+\delta)\left(\dfrac{C_{M_{i-1}}}{C_{M_{i-1}}+C_{i-1}}\dfrac{V_{DD}}{\tau}+r\right)\cdot t_{s_{i-1}}}{\dfrac{V_{DD}}{\tau}+(1+\delta)\cdot r}\ ,\ i\geq 2 \tag{4}$$

From the above expression, the time at which the chain starts conducting, $t_{on}=t_{s_n}$, can be easily obtained. According to the previous analysis, the starting point of conduction can be calculated with very good accuracy for a wide range of input transition times as shown in Fig. 3 which is a comparison between the calculated and the actual time t_{on} obtained from SPICE simulations for a 0.5 micron technology.

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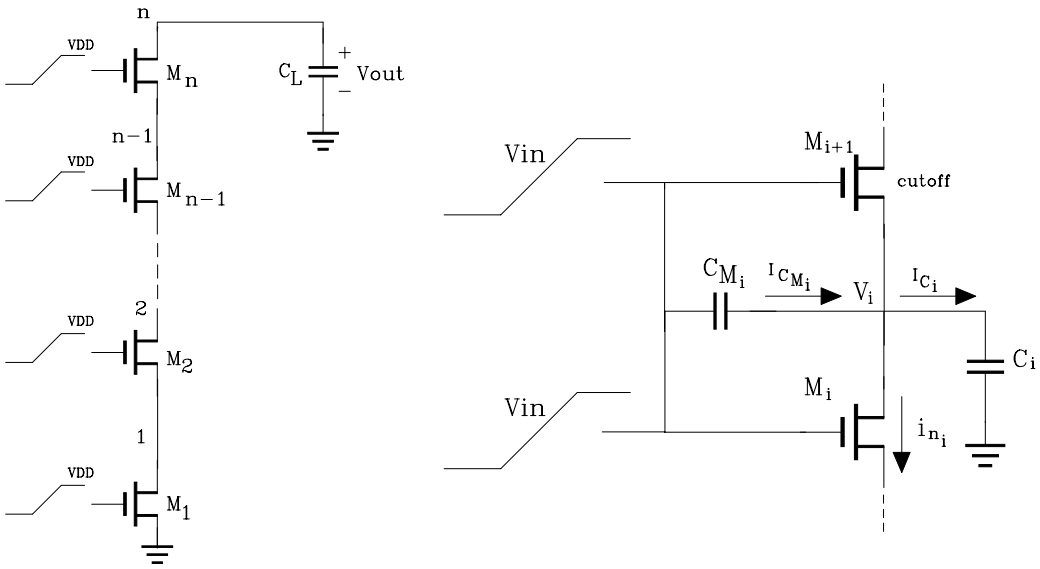
LIST OF CAPTIONS

Fig. 1: (a) nMOS Transistor chain and (b) Currents at node #*i* of the transistor chain during $\left[t_{s_i}\,,\, t_{s_{i+1}}\right]$

Fig. 2: (a) Actual intermediate node voltage waveforms and (b) simplified representation

Fig. 3: Comparison between simulated and calculated starting point of conduction for (a) 4-transistor chain (W=4μm) and (b) 6-transistor chain (W=9μm)



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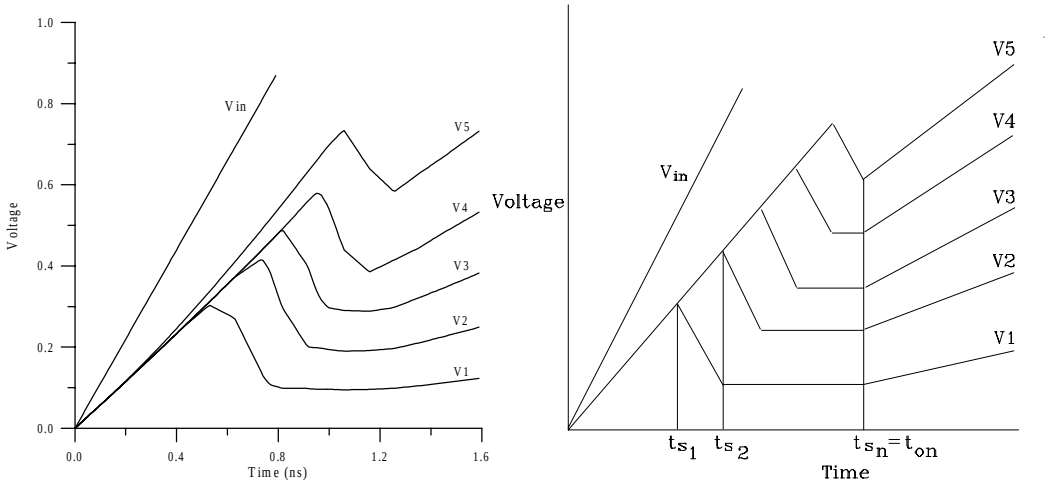

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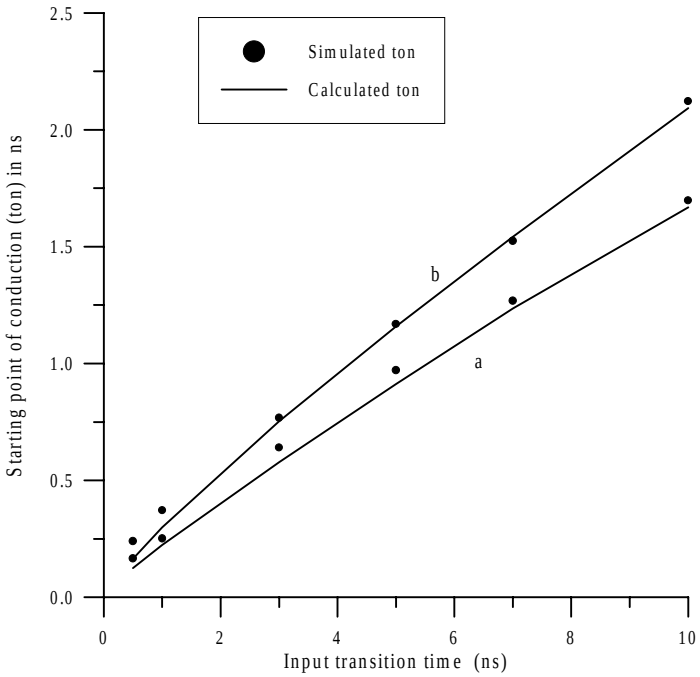

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